TIPHAINE PÉLISSET

DEGRADATION ANALYSIS OF THIN DIE-ATTACH LAYER UNDER CYCLIC THERMAL LOAD IN MICROELECTRONICS PACKAGING

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Kurzfassung

In der Leistungshalbleiterindustrie gelten bereits jetzt hohe Anforderungen an die Zuverlässigkeit der Bauteile. Der Trend bei neuen Technologien geht hin zu höheren Stromdichten bei gleichzeitiger Reduktion der Größe. Zusätzlich steigen auch die Anforderungen an die Zuverlässigkeit und die erwartete Lebensdauer.

Diskrete Leistungshalbleiter versagen auf Grund einer Vielzahl von Mechanismen, wie etwa Korrosion, Elektromigration und thermische Expansion. Die daraus resultierenden Fehlermodi sind unterschiedlich: Riss im Chip, Riss in der Metallisierung oder Abhebung des Bonddrahtes. Der dominierende Fehlermechanismus wird durch den Unterschied im Wärmeausdehnungskoeffizient des Package Materials erzeugt. Der Wärmedehnungskoeffizient liegt innerhalb eines Intervalls von $3 \times 10^{-6}\,\mathrm{K}^{-1}$ bis $50 \times 10^{-6}\,\mathrm{K}^{-1}$, von einem kleinen Wert für Silizium bis hin zu einem großen Wert für die Pressmasse. Zyklische thermische Belastung führt zu zyklischen Spannungen und damit zur Werkstoffermüdung.

Diese Arbeit beschreibt das Werkstoffverhalten und die Materialermüdung von dünnen Lotschichten unter zyklischer Belastung. Ziel ist es, experimentell und mittels Simulation an dieses Thema heranzugehen. Zu Beginn wird sowohl ein Materialmodell als auch eine experimentelle Methode für die Untersuchung des elasto-platischen Verhaltens des Lötverbindung präsentiert. Hierzu werden Finite Elemente Simulation, als auch Wafer Krümmungs Messungen durchgeführt. Für die Beschreibung des Materialverhaltens wird das elasto-viskoplastische Modell von Chaboche herangezogen, dessen Materialparameter mit Hilfe von Monte Carlo Simulationen abgeschätzt werden. Der Vergleich der Simulationsergebnisse mit den gemessenen Spannungs-Temperatur-Kurven zeigt, eine sehr gute Übereinstimmung. Durch die Wahl von geeigneten Randbedingungen konnten die dazu notwendigen Finiten Elemente Modelle auf wenige Elemente reduziert werden.

Im zweiten Schritt wird die Schädigung in der Metallschicht in-situ untersucht, *d.h.* in regelmäßigen Abständen während des zyklischen Testens wird die Metallschicht mit Ultraschall untersucht und analysiert. Diese nicht-destruktive Methode ermöglicht die Beobachtung von Rissausbreitung. Nach dem Test wird die genaue Fehlerursache mittels Cross-Sectioning er-

mittelt. Zwei Modi dominieren: Delamination an der Grenzfläche und Risse innerhalb der Metallschicht. Die Delamination an der Grenzfläche folgt einem Potenzgesetz. Der Einfluss von Geometrie- und Werkstoffparametern wird simulativ - mittels Methoden der linear-elastischen Bruchmechanik - untersucht. Für das Package wird ein zwei-dimensionales Modell verwendet, wobei für die Materialien elastisches Verhalten angenommen und die Struktur zu drei Komponenten vereinfacht wird: Leadframe, Chip und Pressmasse. Für diesen Aufbau werden die Spannungsfelder und daraus die Energiefreisetzungrate bei Rissfortschritt berechnet. Abhängig von der Risslänge verändert sich die Freisetzungsrate, sie erreicht ihr Maximum für eine bestimme Kombination aus Chip und Leadframe Dicke.

Um die Entwicklung der Schädigung genauer zu untersuchen, wurde eine weitere Simulationsmethode angewendet. Diese verwendet ein komplexeres Modell, welches die multiplen Schichten an der Chiprückseite berücksichtigt. Die Delamination der Grenzschicht wird mittels einer Cohesive-Zone Ansatzes modelliert. Zusätzlich wird auch die Veränderung der Temperatur und die plastische Verformung der Metallschichten während der zyklischen Belastung berücksichtigt. Der simulierte Rissfortschritt zeigt den gleichen Trend wie die Experimente. Die Delamination entsteht an den Kanten und wächst in Richtung Zentrum, wobei die Risslänge einem Potenzgesetz in Abhängigkeit der Zyklenzahl folgt. Diese Untersuchungen zeigen, dass sich der Cohesive-Zone Ansatz für die Modellierung von Rissen in dünnen Schichten unter zyklisch thermischer Belastung gut eignet.

Abstract

HIGH reliability is a crucial topic in the semiconductor industry. The main trend for power devices pushes toward higher current density and smaller component size. Additionally, increasing reliability and lifetime are expected.

Discrete power devices are known to fail due to a number of mechanisms, such as corrosion, electromigration or stress migration and thermal expansion. All these failure mechanisms can result in various failure modes, such as chip crack, metalization layer crack or wirebond liftoff. One of the major failure mechanisms is triggered by the difference in thermal expansion of the material of the package. The thermal expansion can range from $3 \times 10^{-6}\,\mathrm{K}^{-1}$ to $50 \times 10^{-6}\,\mathrm{K}^{-1}$ depending whether the silicon or the mold compound are considered. Thermal cycling of these devices results in cyclic stresses in the materials. Under repetitive stress, fatigue of the material occurs.

This work deals with the material behavior of a very thin die-attach alloy as well as its fatigue degradation under thermal cycling. The problem is tackled from two sides, experiment and simulation. First a material model for the studied material is obtained. A methodology to derive the elastoplastic behavior of thin films under thermal cycling is presented. This approach utilizes wafer curvature characterization techniques and finite element simulations. The material behavior is modeled with continuum plasticity. In order to determine the material parameters, Monte Carlo simulations are performed. The validity of the parameter set is assessed by comparing stress-temperature measurements with the simulated results. An adequate choice of the boundary conditions allows keeping the Finite Element model small, which reduces the computational time required due to non-linearity and multiple thermal cycle simulations.

In a second step, the degradation of the layer in-situ, *i.e.* in the package under temperature cycling is monitored, by alternately cycling the device and regularly investigating the degradation using Scanning Acoustic Microscopy. This non-destructive technique allows to monitor crack propagation in the layer. The exact failure mode is then identified by package cross-sectioning. The failure is observed to propagate in two ways, either by interfacial delamination or by in-layer crack formation. The delamination is found to progress as a power law of the number

of cycles. From the simulation point of view, the influence of parameters such as package geometry and material properties is investigated by using Linear Elastic Fracture Mechanics. A two-dimensional model of the package is built, where the materials are assumed to behave elastically and the structure is simplified by considering only the leadframe, the chip and the mold compound. Finite Element simulations yield the displacement and stress fields from which the energy release rate is calculated. Its evolution for various crack lengths is studied. It is found that the energy release rate reaches a maximum for a given combination of chip and leadframe thickness.

A second simulation approach is used where the actual damage evolution is calculated. A more sophisticated model of the structure, encompassing the multiple backside layers usually present at the back of the semiconductor chip is simulated. The delamination is modeled using a cohesive zone approach. Temperature cycling and plasticity of the backside metalization layers are taken into account in the simulation. The crack propagation is shown to follow the same trend as observed in the experiment, *i.e.* delamination growing from the edges propagates toward the center and the crack length is a power law of the number of cycles.

It has been shown that the cohesive zone approach is an appropriate technique to model degradation of the thin layers of the package under cyclic thermal loading conditions.

Contents

1

Introduction

In this chapter, a short introduction to power electronics packaging and reliability issues in discrete packages is given. Then a detailed description of the device used as test device is made for further reference. A review on the degradation of thin layers as well as currently used modeling approaches is given. Then the objectives of this thesis are stated along with its structure.

1.1 Power electronics packaging

A power electronics system can be defined as an efficient energy conversion means using power semiconductor devices [1]. They are used, for instance, in the wind energy industry, motor drive applications, power supply for server farms *etc.* Power electronics has invaded our daily life, notably in the field of power supply devices. A mechanical converter that a few decades ago occupied several cubic meter fits nowadays in a cubic millimeter volume, while ensuring the same function. Power semiconductors employed in electronic systems include power switches and rectifiers (diodes). An ideal switch applies power to a load when a voltage is applied to its control terminal. It should be able to turn on and off instantaneously. Additionally it should have an infinite impedance when turned off so that zero current flows to the load. It should have zero impedance when turned on so that the on-state voltage drop is zero. Another ideal

characteristic would be that the switch input consumes zero power when the control signal is applied [2]. In practice, switching time is limited by the parasitic capacitances of the component, *i.e.* from the semiconductor device and its package. Usually, the largest power dissipation occurs during switching. Parasitic inductance, for instance due to the presence of multiple wirebonds, might lead to over-voltage, potentially dangerous for both the load and the switch. Power devices handle power levels from the microwatts to the megawatts. Power switches are found either as discrete devices, *i.e.* one device cased in a single package or as modules, which consists of a single package of several devices with a power capability above that of integrated circuits [3].

The main development trend of power devices focuses on increasing the power rating, *i.e.* the maximum power to be used with the device, and current density while decreasing the component (and/or chip) size and improving the overall device in terms of losses, robustness and reliability under normal and fault conditions [1, 4, 5]. Thermal considerations like device losses, cooling and maximum operating temperature determine the physical limits of a power electronic circuit. To handle the large heat flux density, high thermal conductivity is required.

1.1.1 Overview of discrete device packages

The housing of the semiconductor chip plays a major role in enhancing the device lifetime, as it provides mechanical support and protection from the environment, power and signal transmission as well as thermal dissipation. The overall performance of a discrete device is not only determined by the processing technology but also affected by the packaging technology. Nowadays, the price contribution of the package might be as large or even larger than the chip price. [2] Globally, all these packages are built based on the same principle. The chip is soldered to a copper base plate, the leadframe, which often features one of the contacts of the device. Wirebonds are used to connect the front side of the device to external leads, themselves soldered to the Printed Circuit Board (PCB). The device is encapsulated into a plastic material made of a mixture of epoxy and silica particles. An example of such a package and its inside components is shown in Fig. 1.1.

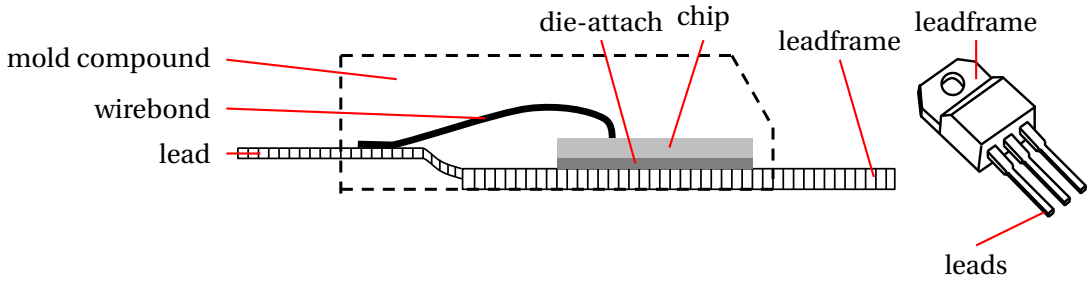


Figure 1.1: Transistor-Outline (TO) package with a cross-section view and the full view.

Power semiconductor discrete device packages are divided in two categories: through hole and surface mounted devices as shown in Fig. 1.2. Surface mounted devices allow for increased circuit density (mounting on both sides of the PCB) and improved electrical performance (lead parasitic resistance and capacitance are eliminated) [6]. For through hole devices, Dual-In-Line (DIP) package, Transistor-Outline (TO) package and Pin Grid Array (PGA) are the more common ones, while Small Outline (SO) package, Quad Flat Pack (QFP) package, Small Outline Transistor (SOT) package and Plastic Leaded Chip Carrier (PLCC) package are the typical surface mount packages. Both through hole and surface mount devices are mounted on a PCB. Surface device mounting is beneficial to the resulting circuit as it decreases the inductance.

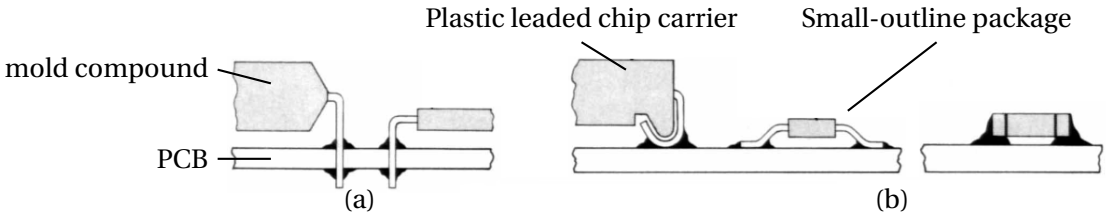


Figure 1.2: (a) Through hole technology (b) Surface Mount Technology. Extracted from [7].

1.1.2 Reliability of power semiconductor devices

Fundamentals of reliability

Reliability is the "ability of a system or component to perform its required functions under stated conditions for a specified period of time" [8]. The requested lifetime for power electronics systems is usually about 20 years. The bathtub curve is used to describe life expectancy (Fig. 1.3). Three different regions are distinguished. In the first region, early failures occur. The devices failing in this region are usually screened by a technique called burn-in, where the devices are subjected to a given set of operating conditions and tested for a given time. After burn-in, their electrical parameters are measured and all devices having drifted out of specifications are withdrawn. Random failure and wear-out are two stages of failure that occur at the customer side. They result from normal usage of the device. Random failures might occur due to external stress such as overvoltage or electrostatic discharge. The wear-out region results from the aging of the device, when phenomena such as electromigration begin to be significant. [9–11]

Thermal management is a reliability issue in power semiconductors as operation at elevated temperature can result in both degraded performances and reduced lifetime [2]. The parameter to control is the maximum junction temperature. The junction temperature is a function of the electrical characteristics of the device itself, as well as the package employed. Package ther-

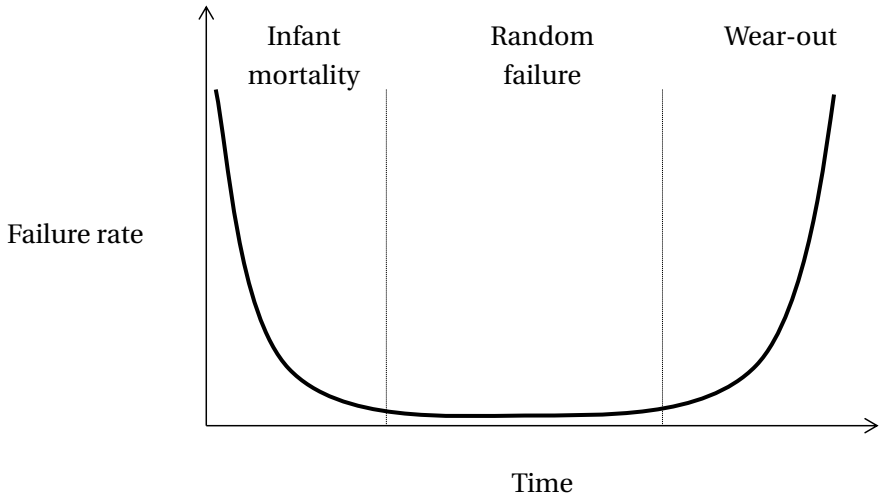


Figure 1.3: Bathtub curve with the three regions that are usually identified.

mal properties determine its ability to extract heat from the die. On-resistance is an important parameter of power semiconductor devices because it determines the power loss and heating of the component. The lower the on-resistance, the lower the device power loss and the cooler it will operate.

Accelerated testing

It is impossible to test the reliability of power devices under field conditions, as a test would last as long as the required service lifetime. As a result, accelerated tests are defined which are widely accepted as representative data for the device reliability. Failure criteria are defined which allow a certain increase relative to specification limits or initial measured values. Since the accelerated tests are supposed to simulate the stress applied in the total service lifetime, the specified values are permitted to be exceeded with a given tolerance. A large variety of tests and test conditions exists, which assemble temperature, humidity and storage, under on or off state of the device. They aim at evaluating the mechanical stability and the electrical connections.

A large number of tests is used. A few of them are briefly described here. Temperature Cycling (TC) consists of cycling devices in a thermal chamber. The devices are not electrically connected. The main failure mechanism is the thermal mismatch. High Temperature Reverse Bias (HTRB) consists in biasing the device in a specific condition at elevated temperature for a large number of hours and monitoring the leakage current of the device. Failure will occur when the leakage reaches such a high level that the power dissipation causes the device to go into a thermal runaway. Low Temperature Storage Life (LTSL) checks the ability of a device to withstand low temperature (−65 °C) for a large number of hours. The devices are not electrically

connected for this test. Intermittent Operating Life (IOL) consists of turning the device on and off alternately. The device heats up during cycling on because of power dissipation and cooled down during cycling off due to the removal of the applied power. Failure occurs when thermal fatigue of the wirebond or die-attach causes the device's electrical parameters to increase beyond the specification values. Standards describe the test conditions and setup (AECQ101, JEDEC). [12]

Failure mechanisms in discrete devices

Numerous failure mechanisms may come into play in the complex structure of a power component. Failure mechanisms related to semiconductor physics, such as mobile ions in the oxide layer or crystal defect density of the bulk material, are critical from the device point of view. Failure mechanisms related to environment, like electrostatic discharge or overvoltage have to be considered in device handling and use. Failure mechanisms and the possibly observed failure modes related to the material have a significant impact on reliability as well. A few of the possible failure mechanisms are described here.

Corrosion is the degradation of metals by chemical reaction with their environment. Usually, it consists of electrochemical oxidation of metals in reaction with an oxidant such as oxygen. Corrosion degrades the material properties, including their mechanical strength or electrical conductivity. Corrosion failures are twofold: (i) bonding pad corrosion occurs when the die passivation does not cover the metalization in the bonding pad locations, (ii) internal corrosion (away from the bonding pads) is attributed to weakness or damage in the die passivation permitting moisture to reach the metalization. [13]

Electromigration is a stress assisted diffusion in the presence of an electric field. It typically occurs in metallic interconnections with high current densities. Thin metal lines usually carry higher current densities than bulk metal wires without melting due to the Joule effect because of the presence of surrounding dielectric materials, which act as heat sinks. Moving electrons transfer significant momentum to the stationary metal atoms, inducing their diffusion in the direction of electron transport. Electromigration results in loss of current carrying capability due to the formation of voids and possible electrical short circuits. [13, 14]

Stress migration describes the motion of metal atoms under the influence of mechanical stress gradients, built up by grain growth and thermal expansion. Such motion occurs when the yield point of the metal is overcome. Voids nucleate and grow at grain boundaries and geometrically sharp corners. The electrical resistance rises progressively till the metal line fully loses its current-carrying capability. [13, 14].

Thermal expansion is a major issue in packaged devices which results in various failure modes

such as wirebond lifting, die-attach and metalization fatigue or metalization reconstruction. It induces for instance wirebond lifting. Due to the change in length of the wirebond, the welded connections of the bond feet move and become damaged. In case of several wirebonds, the damaging of one wirebond induces larger current densities in the other ones, thus accelerating their degradation by other failure mechanisms. However in practice a pure circuit interruption is very rare. Thermal expansion combined with thermal cycling induces die-attach and metalization fatigue. The difference in thermal expansion coefficients of the material layers induces an alternating stress in the die-attach and the other metalization layers. The higher the temperature difference becomes, the more the metal layers are strained. Die-attach fatigue leads to an increase in electrical resistance and in chip temperature, which in turn causes higher losses and higher temperature gradients in the device. It results in a global acceleration of the aging process. Additionally, plastic deformation of the metalization layers might result in the extrusion of single grains. Significant grain extrusion leads to voids in the metalization layer. This phenomenon, called reconstruction is an aging process induced by power cycling. Changes in the chip metalization gradually increases the chip resistance causing additional losses, higher temperature gradients and degraded wirebond adhesion, thus accelerating the failure process. [11, 15, 16]

1.2 Test device

This work deals with degradation of the die-attach due to thermal fatigue. The test device is a diode. Its electrical characteristics will be used in the experimental work. From the electrical point of view, a diode lets the current flow when the voltage drop at its terminal exceeds its forward voltage. The forward voltage depends on the material from which the diode is fabricated, either silicon or silicon carbide. The forward voltage is temperature dependent. The diode is packaged in a classical TO package with two leads. The chip is soldered to the leadframe by means of a thin layer, obtained by diffusion soldering.

1.2.1 Die-attach layer

Thin layer for the die-attach is of interest when the device performance is limited by the electrical and thermal properties of the package. A thin layer as die-attach, made of a highly conductive material, improves the thermal performance of the device by increasing its ability to dissipate heat. Additionally, the electrical performance is improved as the parasitic electrical resistance of the package is decreased, which might lead to a faster switching of the device. Such a die-attach layer is highly relevant for devices allowing higher power dissipation, such as silicon carbide based devices. [17]

1.2.2 Diffusion soldering principle

Diffusion soldering brings two low melting point materials into contact under moderate temperature and pressure in order to realize a connection. The low melting point material melts at the temperature of the process. Due to the mechanical force applied between the two systems, a good mechanical contact between the surfaces is ensured. Diffusion of the metallic atoms occurs, resulting in the formation of a new phase whose melting point (T_m) is much higher than the process temperature. The principle of diffusion soldering, also called transient liquid phase bonding is described in Fig. 1.4 [18].

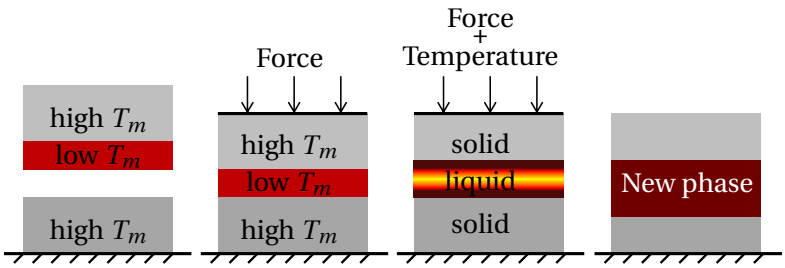


Figure 1.4: Principle of the diffusion soldering process.

In the case of the AuSn-Cu system, a thin layer of AuSn is deposited on the chip's backside. The chip and leadframe are brought into contact under a small force to ensure a mechanical contact that is as conformal as possible. The system is heated up to 360 °C, where the AuSn layer is in the liquid phase. The copper atoms diffuse from the solid leadframe into the AuSn layer, resulting in a progressive change of composition. A new phase is formed, which has different mechanical and physical properties than the initial materials. [19]

1.3 Degradation modeling

A number of methods from domain like large structure, composite materials or bulk degradation are available to model the degradation of materials. Some methods are based on the calculated stress and strain fields: they predict the possible failure location in a structure. Other methods, based for instance on damage mechanics, introduce a damage variable d, which evolves according to the loading situation.

1.3.1 Damage indicators

Fatigue modeling using damage indicators consists of four steps. First a suitable constitutive model must be chosen. Appropriate assumptions need to be made for constructing the constitutive equations. After calibrating the corresponding parameters of the constitutive model, the stresses and strains inside the component can be calculated, *e.g.* by means of a Finite Element (FE) analysis. Third the simulated values are used as input to a model predicting the number of cycles to failure. These simulated results must then be tested against actual experimental data. The stress-based models are applicable when a force is applied to a component, causing strains (vibration, shock...). The strain-based models are to be applied for strain controlled loading: a typical application is thermo-mechanical fatigue due to thermal expansion mismatch. Energy-based models key the energy dissipated in the material during loading. A critical strain or energy value is provided for an empirical fatigue model that theoretically predicts the number of cycles to failure. The Coffin-Manson model is one widely used approach [20]. In this kind of model the initiation phase of the crack is not considered. Additionally, the progressive material degradation during lifetime is not taken into account either. Another major limitation of these models is the fact that they are geometry dependent and as such not transferable to other packages. Thus they are not material models but empirical models. Nevertheless, such an approach has been successfully applied to solder joint in microelectronics. [21–24]

1.3.2 Fracture mechanics

Fracture mechanics approaches of degradation consist of calculating given fracture parameters from the stress and strain fields. Depending whether this parameter exceeds the experimentally determined critical limit for the material, the crack will propagate. This approach does not consider the initiation phase of the crack, the simulation model must assume a preexisting crack. The Paris law [25] can be used to model the propagation phase of the crack, for instance depending on the amplitude of the energy release rate during one cycle. This approach can be used to compare loading situations or geometries, if it can be assumed that the same failure modes occur. [26]

1.3.3 Damage mechanics approach

Damage mechanics incorporates an additional variable in the constitutive model, a damage state variable d, that has its specific evolution law. This variable represents all the phenomena occurring in the material during degradation, from microcracking to void formation and coalescence depending on the type of failure. This kind of model represents initiation and propagation of the damage. For a bulk material, it is implemented as a reduction of the effective stress

that the material can bear. However, it is not suitable for modeling interface behavior. [27]

1.3.4 Cohesive zone

The Cohesive Zone (CZ) approach is a combination of damage mechanics and fracture mechanics. It can be applied to the bulk as well as to the interface. The fracture toughness of the layer is incorporated into the Traction-Separation Law (TSL), which describes the progressive separation of the crack faces. The Cohesive Zone (CZ) approach is widely developed for monotonic loading, where the load is applied once and never withdrawn. However, such models cannot be directly used in the case of cyclic loading as they do not account for fatigue damage. It is possible to develop and implement models including a damage parameter as internal variable, which already evolves during subcritical loading, thus giving rise to a fatigue effect.

All these models require material data to be implemented. A large experimental effort is required. However, with model based on cohesive zone or damage mechanics, one is sure that the developed and calibrated model will be transferable to other geometry, if the failure mechanism is identical, as these models represent the behavior of the material or the interface between two materials, without geometry influence.

1.4 Objective of the thesis

Maintaining the integrity of the die-attach is one of the major challenges in package technology. In the case of power semiconductors, the die-attach layer might be used both as electrical and thermal connection, enabling the dissipation of most of the heat. It is a crucial layer in the package. One possibility to improve its thermal and electrical capabilities is to change the material and reduce the thickness. However, as with every new material introduced in the package a detailed knowledge of the behavior is needed. The crack propagation rate under thermal fatigue of such a layer in a full package is expected to differ significantly from the known form of crack propagation in larger structures. The relevant issue here is thin film behavior, with the possible limit of the validity of the continuum mechanics. We investigate possible methods that are widely used in bulk materials on a larger scale to model degradation of layered structures in the special case of the previously described device. The results are qualitatively compared to experimentally investigated test devices to evaluate whether the method is valid and applicable in this specific case. The general question remains whether alternative simulation techniques might be better suited in the semiconductor industry to evaluate the reliability of packaged devices. But this has not been the focus of this thesis.

1.5 Structure of the thesis

The first step of this work aims at establishing a basic understanding of the mechanical behavior of the material formed by diffusion soldering of copper in gold-tin. The material behavior is evaluated by using a curvature technique measurement. The observed behavior is reproduced by a model such that the actual behavior can be used in the subsequent package simulations. The method and results are reported in Chapter 2.

Test devices in a typical package for a discrete device, the TO package, soldered by diffusion soldering are investigated under temperature cycling. The monitoring of the damage progression is made using Scanning Acoustic Microscopy (SAM). Thus data about crack growth in such a device are collected in order to evaluate the typical failure evolution. Failure modes are identified by device cross-sectioning. The test setup and results are reported in Chapter 3.

Using Linear Elastic Fracture Mechanics (LEFM) and a simplified package structure the influence of geometry and relative material properties are investigated by Finite Element (FE) simulations. The objective is to determine the most influential parameter for degradation using this approach, see Chapter 4.

In Chapter 5, the crack growth rate is investigated by using a cohesive zone approach in a two-dimensional structure by FE simulations. The results are compared to the experimental results of Chapter 3.

Chapter 6 summarizes the findings of this thesis and the main results are outlined. Additionally, further topics are discussed that may lead to a better understanding and more accurate prediction of semiconductor package lifetime.

2

Material characterization

A methodology to derive the elastoplastic behavior of thin films under thermal cycling is presented. This approach utilizes wafer curvature characterization technique and finite element simulations. The material behavior is modeled with continuum plasticity and includes Bauschinger effect and cyclic behavior. In order to determine the material parameters, Monte Carlo simulations are performed. The validity of the parameter set is assessed by comparing stress-temperature measurements with the simulated results. This methodology is applied to the various thin metalization layers to determine the material model parameters. This approach is efficient due to the use of a single column of elements in the FE simulations, which reduces the computational time required due to non-linearity and multiple thermal cycle simulations.

2.1 Experiments

2.1.1 Wafer curvature technique

The curvature measurement technique allows studying the thermomechanical behavior of thin films under thermal cycling. A bilayer, made of a thin film deposited onto a relatively thick substrate (Fig. 2.1), is thermally loaded. Substrate deformation arises from the difference between

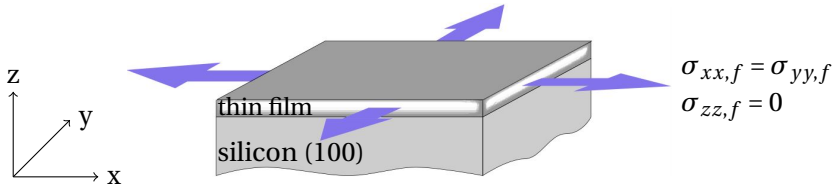


Figure 2.1: Typical sample. A bilayer, made of a thin film deposited onto a relatively thick substrate, is thermally loaded. The film in-plane normal stresses $\sigma_{xx,f}$ and $\sigma_{yy,f}$ are equal while the out-of-plane normal stress $\sigma_{zz,f}$ vanishes.

the thermal expansion coefficients of film and substrate. Under certain conditions, the deformation is spherical and can be described by a single parameter, the curvature κ. It is interpreted in terms of stress by means of Stoney's formula. It allows determining an average film stress σ_f without involving the film material properties:

$$\sigma_f = M_s \frac{h_s^2}{6h_f} (\kappa - \kappa_0), \tag{2.1}$$

where the indices s, f refer to the substrate and film respectively, h is the layer thickness, κ_0 the curvature of the bare substrate and M_s the substrate biaxial modulus. For a (100) silicon substrate, the biaxial modulus is given by [28]:

$$M_s = \frac{1}{s_{11} + s_{12}}, \tag{2.2}$$

where s_{ij} are the compliance components of the substrate material. In the case of a film deforming elastically over the studied temperature range, the thermal strain ε_{th} needed to fit the film to the substrate is:

$$\varepsilon_{th} = (\alpha_s - \alpha_f)(T - T_{dep}), \tag{2.3}$$

where $\alpha_{s,f}$ are the thermal expansion coefficients of the substrate and film respectively, T is the current temperature and T_{dep} the film deposition temperature.

The substrate material is chosen such that its mechanical properties are well known and it deforms elastically in the temperature range of interest. In practice, silicon wafers are often chosen as being comparatively cheap wafer with well optimized deposition processes for the films. Several methods can be used for thin film deposition. They are classified in two categories: Physical Vapor Deposition (PVD) and Chemical Vapor Deposition (CVD). PVD are methods such as evaporation or sputter deposition, where the film material is taken away from a material target by inert atoms and brought onto the silicon wafer surface where they form a film. In CVD, ionized atoms of the material to be deposited are brought in a reaction chamber in the gaseous form. In contact of the wafer, the ions are adsorbed by the wafer lattice. Chemical byproducts result from CVD. During both CVD and PVD, the wafer is usually slightly heated

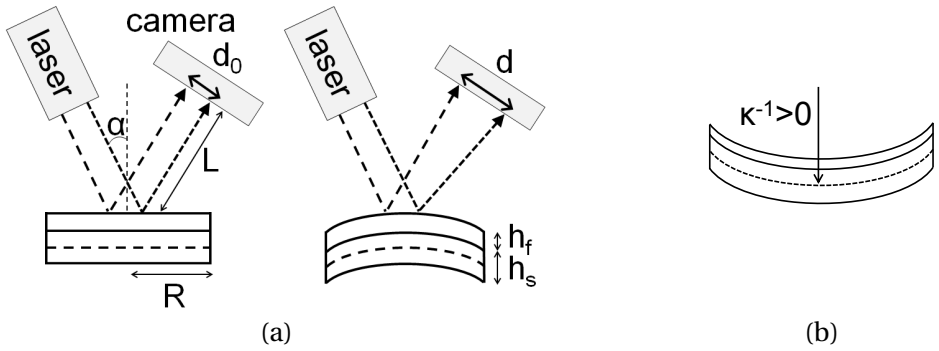


Figure 2.2: (a) System schematic. The dashed line depicts the substrate neutral plane. The initial beam spacing d_0 is obtained by means of a flat mirror. The instantaneous beam spacing d is proportional to the curvature. (b) Curvature sign convention, the upper layer is the film.

(50 °C) to activate surface diffusion of the atoms. The control of the process parameters such as temperature and gas flow rate influence both the grain size and the film texture. Curvature sample size can go from a full wafer (250 mm diameter in KAI tool) to a sample of a few square centimeters. As it will be discussed in the next section, the only requirement is that the in-plane dimension of the sample, for instance its diameter R, is much larger than its thickness ($R >> h_s >> h_f$). Misfit stress due to non-equilibrium film growth and thermal stress make up the total stress of a thin film constrained by a rigid substrate. Tensile growth stress arises from various sources such as non-equilibrium film growth, grain growth, excess vacancy annihilation, grain boundary relaxation or grain boundary void shrinkage [29].

The sample is placed in a thermal chamber and heated using a lamp array. It is set such that the temperature distribution is uniform in the in-plane direction. The temperature of the sample is assumed to be uniform in the thickness direction. The curvature change under thermal loading is monitored by a laser array. The laser array beams are reflected by the sample surface and detected by a CCD camera, as shown in Fig. 2.2a. The change of the beam spacing is recorded. A linear relationship exists between the beam spacing d and the substrate curvature κ. Using the curvature convention given in Fig. 2.2b, the beam spacing is linked to the curvature by [30]:

$$\kappa = -\frac{\cos\alpha}{2L}\frac{d-d_0}{d_0} \tag{2.4}$$

where α is the incidence angle of the laser beam array on the substrate, L is the sample-detector distance, d is the beam spacing and d_0 is the beam spacing for a flat mirror. The parameters α and L are obtained by calibration with a mirror of known curvature. Their magnitudes are: $\alpha \approx 5°$ and $L \approx 50$ cm. The tool detects curvature changes of 5×10^{-5} m^{-1}. It has a precision of 11×10^{-5} m^{-1}. The measured values are accurate within 47×10^{-5} m^{-1} compared to their actual value. From a tool point of view, the substrate curvature has to be large enough compared to the tool accuracy to minimize the relative error on the measurement. From an interpretation

point of view, the curvature must be small enough such that Stoney's equation (small strain approximation) is still valid. For a given film and substrate material, the stress sensitivity is related to the curvature. The larger the curvature, the better the sensitivity. For a 1 µm-thick aluminum film deposited onto a 520 µm-thick (100) silicon substrate with properties given in Tab. 2.1, submitted to a temperature change of 10 °C, the elastic strain is 2.05×10^{-4}, the induced curvature is $2.63\times10^{-3}\,\mathrm{m}^{-1}$ giving a stress of 21.4 MPa. The stress resolution for this sample reaches 0.4 MPa. The accuracy is 3.8 MPa.

Table 2.1: Material properties for aluminum [14] and silicon [14, 31]. The Young's modulus for aluminum is the arithmetic mean between the Young's modulus for the ⟨111⟩ and the ⟨100⟩ direction.

Properties	Aluminum	Silicon
Young's modulus E (GPa)	70	130
Poisson ratio ν	0.33	0.28
Coefficient of thermal expansion α (K^{-1})	23.6×10^{-6}	3.1×10^{-6}

Thermal stress arises from the difference in coefficient of thermal expansion between film and substrate. In order to induce plastic deformation during thermal cycling, a large difference in thermal expansion between film and substrate is needed.

2.1.2 Stoney's formula

Stoney's formula is the central relation connecting substrate curvature to film stress. It can be derived either through a mechanical equilibrium approach or by an equivalent elastic energy minimization approach [14]. A number of assumptions is required to derive it [32]:

(1) Both the film thickness h_f and the substrate thickness h_s are uniform.

(2) The film is much thinner than the substrate: $h_f \ll h_s$.

(3) Both the film and substrate thickness are small compared to a characteristic lateral dimension R (e.g., system radius): $h_s, h_f \ll R$.

(4) The strain and rotations of the plate system are infinitesimal so that all the assumptions of small strain geometrically linear theory apply.

(5) The film and substrate material are homogeneous, in-plane isotropic and linearly elastic. Some of these assumptions can be relaxed. The substrate must be in-plane isotropic, such as a (100) or a (111) silicon substrate, to ensure a symmetrical deformation. It must deform elastically over the tested temperature range. For polycrystalline film without texture, the isotropy assumption holds. For polycrystalline film with strong crystallographic texture, the film biaxial modulus should be adapted. Nix [33] gives the appropriate biaxial modulus values for cubic single-crystal films. Stoney's formula allows to derive an

average film stress, which can vary locally due to microstructure. The film is allowed to deform plastically as the system behavior is dominated by the substrate.

(6) The in-plane normal stress components are equal while the out-of-plane normal stress and all shear stress components vanish far from the edges.

(7) The curvature components are equibiaxial and the twist curvatures are zero.

(8) All stress and curvature components are spatially constant over the plate surface. This assumption is only approximated in practice.

A thin film is bonded to an elastic substrate. The film has a misfit strain with respect to the substrate. This strain may arise from thermal expansion effects, epitaxial growth or deposition process. The stress associated with the misfit strain induces curvature. The misfit strain is assumed to be an isotropic extension or compression in the plane of the interface. In most practical situations, the thickness of the substrate greatly exceeds the thickness of the film and the film stiffness is lower than the substrate stiffness in which case the following relationships hold:

$$\kappa = 6\frac{h\,m}{h_s}\varepsilon_m \tag{2.5}$$

$$\sigma_f = \frac{h_s M_f}{6hm}\kappa \tag{2.6}$$

where $h = h_f/h_s$ and $m = M_f/M_s$, σ_f the in-plane stress of the film and ε_m the misfit strain. The misfit strain is thermal strain in this work.

Relative film-substrate thickness

Stoney's formula relies on a number of assumptions that may not always be verified. Here, the limits of applicability of the thin film approximation are reviewed. When the film thickness is comparable to the substrate thickness, the curvature depends significantly on the film material properties. Comparing the curvature obtained by violating the assumption of thin film with Stoney's approximation one obtains [34]:

$$\frac{\kappa}{\kappa_s} = \frac{1+h}{1+4\,h\,m+6\,h^2\,m+4\,h^3\,m+h^4\,m^2} \tag{2.7}$$

where κ_s is the curvature obtained from Stoney's equation. The relative error associated with using Stoney's formula is $(\kappa-\kappa_s)/\kappa$. Fig. 2.3 depicts the relative error between the first order Stoney's approximation with the extended solution for thick films as a function of thickness ratio $h = h_f/h_s$ parameterized by the ratio of film and substrate moduli $m = M_f/M_s$. For $h_f/h_s \leq 6\times10^{-3}$ and modulus ratio ranging from 0.1 to 2.5, Stoney's formula is accurate within 6 %.

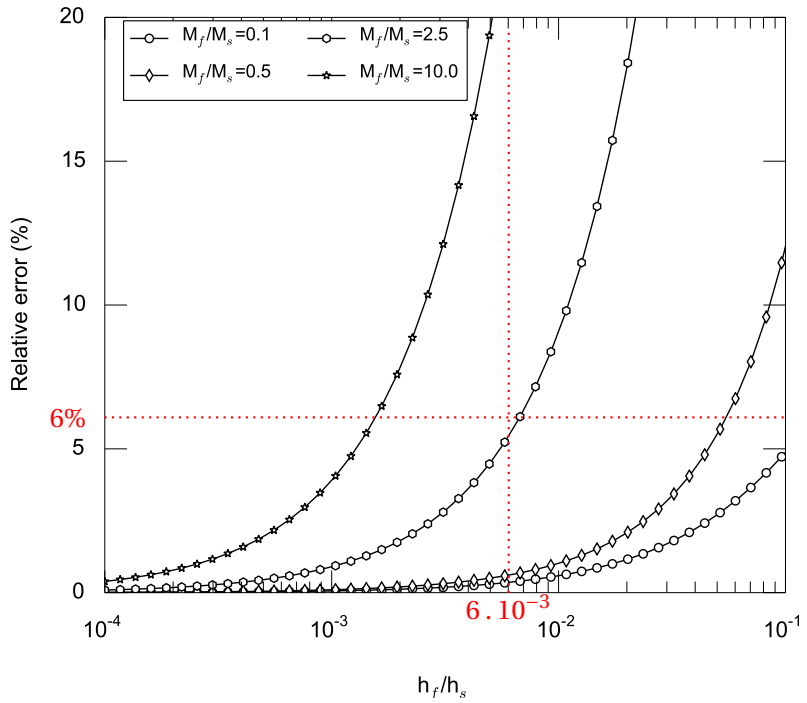


Figure 2.3: Relative error of Stoney's curvature compared to the curvature extended for thick films. For $h_f/h_s = 6 \times 10^{-3}$ and modulus ratio ranging from 0.1 to 2.5, Stoney's equation is accurate within 6% of the h_f/h_s curvature.

Multilayer with small total thickness

To extract the stress of a single layer when only the measurements from the multilayer system are available, two correction methods are available. The layers whose contribution should be removed can be deposited on both sides of the wafer to compensate for the induced curvature. Or the multilayer sample and each bilayer sample can be measured separately and the curvature of the one layer that could not be measured recalculated. [35]

Hsueh [36] demonstrated that different layers with small total thickness h_f contribute independently and additively to the curvature of the system:

$$h_f = \sum h_{f,i} \ll h_s \tag{2.8}$$

$$\kappa = \sum \kappa_i \tag{2.9}$$

$$\sigma_f h_f = \sum \sigma_{f,i} h_{f,i} \tag{2.10}$$

where h_f is the sum of the film thickness $h_{f,i}$ of the i-th layer, κ is the curvature of the multilayer, κ_i is the curvature contribution of the i-th layer. The thermal strain induced in the i-th

layer is:

$$\varepsilon_{m,i} = (\alpha_s - \alpha_{f,i})(T - T_{dep}) \tag{2.11}$$

where T_{dep} is the deposition temperature of the film, T is the current temperature, $\alpha_{s,f}$ are the coefficients of thermal expansion of substrate and film, respectively. All the films are assumed to be deposited at the same temperature. According to the analytical result, the order of deposition of the layers has no importance. This superposition principle will be used for stress calculation of complex stacks.

Edge effect

Near the edges of the film, the plane stress assumption for the film no longer holds. Shear stresses will exist. However, their magnitudes decay rapidly with distance from the edge and become typically negligible for distances greater than $5h_f$ [29]. It imposes a restriction on the minimum sample size. Here square samples of side about 4 cm are used.

From this analysis, it results that for the film thickness and material considered here, the assumptions are fulfilled and the use of Stoney's formula introduces a relative error of about 6 % percent.

2.1.3 Samples preparation

Aluminum

Aluminum thin films with four different thicknesses of 0.19, 0.63, 1.00 and 1.93 µm respectively, are deposited by sputtering at room temperature on a (100) oriented, 520 µm-thick silicon wafer, covered with a 19 nm thermally grown silicon oxide layer to avoid interdiffusion. The oxide layer can be neglected in stress calculations as it is grown on both sides of the wafer. The curvature induced by the presence of a layer on one side of the wafer can be compensated by the deposition of an identical layer on the other side, resulting in zero total curvature induced by these layers [35]. The samples were thermally cycled in air between 25 °C and 450 °C at a heating and cooling rate of 10 °C min^{-1}. In practice, the cooling rate is lower than 10 °C min^{-1} below 100 °C as natural cooling is used. The absolute stress value in the film is obtained by measuring the bare substrate curvature after film removal or by measuring the system by X-ray diffraction. More details about aluminum sample preparation and measurements can be found in the original work [37].

Solder

The solder system under investigation consists in a gold-tin (AuSn) layer brought in contact with a copper (Cu) layer, as shown in Fig. 2.4. The AuSn layer is in such proportion that it melts around 280 °C (about the eutectic composition) as shown on Fig. 2.5b. The system AuSn-Cu is brought to 360 °C for 2 min under a protecting atmosphere of forming gas N_2H to prevent oxidation of the copper. At 360 °C, the AuSn layer is fully melted, which allows fast diffusion of Cu atoms into the AuSn melt. Due to the diffusion, the composition of the melt changes progressively until it reaches a composition at which it is back to the solid state. The newly formed phase, reported to be $Au_2Cu_6Sn_2$ by Etschmaier [19], is solid at 360 °C and corresponds to the so-called phase B in Fig. 2.5b. Upon heating phase B, it will undergo a solid phase transformation to phase A and starts melting around 550 °C.

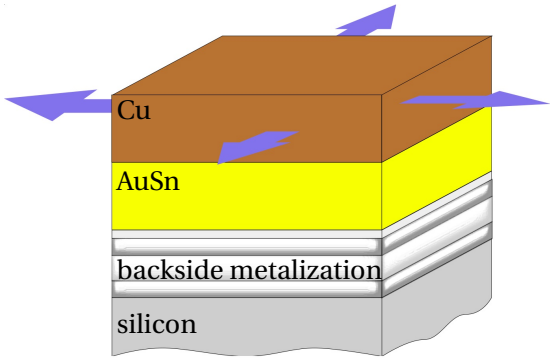


Figure 2.4: AuCuSn sample before diffusion. Backside metalization layers consist in adhesion and barrier layers.

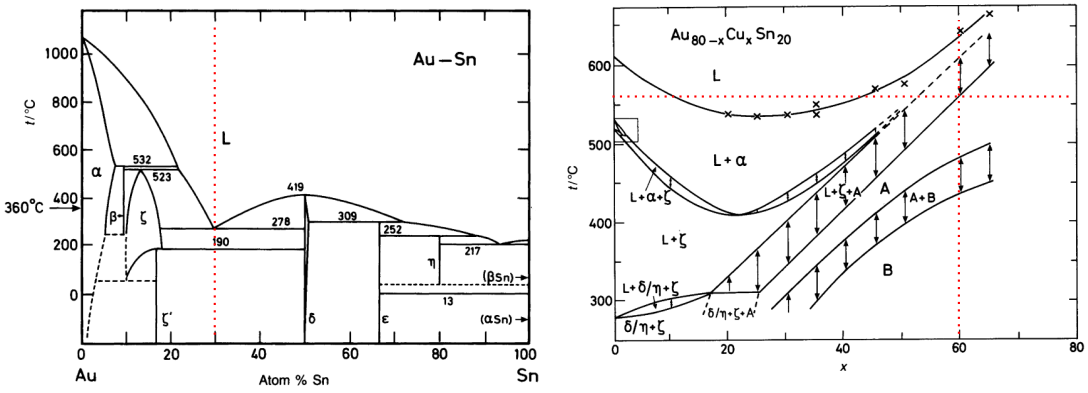
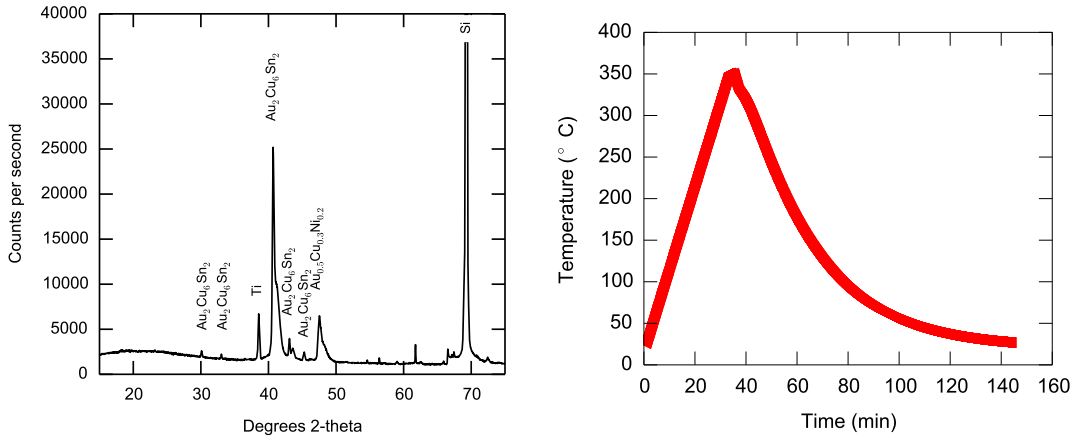


Figure 2.5: (a) Phase diagram for the binary system AuSn and (b) for the ternary system AuSn-Cu. The phase relationships are reported for $Au_{80-x}Cu_xSn_{20}$ where x is in atom percent. Taken from [38]

Manufacturing of the solder sample consists in successive sputtering of metal layers on the silicon wafer. The uppermost layer being the AuSn layer, followed by electrodeposition of a cop-

per layer. According to background work, the diffusion system AuSn on Cu forms a $Au_2Cu_6Sn_2$ phase [19]. To avoid further diffusion of gold in the silicon substrate and enhance adhesion, various adhesion and barrier layers are used. Two version of the sample are built. One version consists in only the backside metalization layers, without AuSn and Cu. The second version consists in the full stack, deposited on a 700 µm thick silicon wafer. The two types of sample are submitted to an identical thermal history. The first cycle consists in heating from room temperature up to 360 °C with a ramp rate of 10 °C min^{-1}. The samples are held at 360 °C for 2 min before being cooled down. The temperature cycling is performed under forming gas atmosphere to prevent copper oxidation. Then cycling between room temperature and 450 °C is done. If the two samples have the same temperature history, then the stress-temperature curves of the solder phase can be calculated using the superposition principle. Fig. 2.6 shows a X-ray diffractogram of a sample annealed according to the previous paragraph. The peak pattern allows to identify a $Au_2Cu_6Sn_2$ phase, as expected from literature [19]. The presence of several peaks for this phase shows that it forms as a polycrystalline layer. An intermetallic phase with nickel is found. It points out the presence of a vertically layered structure thus the assumption of layer homogeneity might not be valid. In this work, the layer structure is not studied in detail.



(a) (b)

Figure 2.6: (a) X-ray diffractogram of the backside metalization after 2 min annealing at 350 °C. The peak pattern allows to identify the $Au_2Cu_6Sn_2$, which is present in a polycrystalline state. Courtesy of Prof. Halwax. (b) Temperature profile for reaction.

Titanium

Titanium is a metal which undergoes an allotropic phase transformation at a temperature higher than half its melting point. It transforms from a closed-packed hexagonal crystal structure to a body-centered cubic crystal structure. The exact temperature of transformation is

strongly influenced by the presence of interstitial and substitutional elements. It is approximately 880 °C. Titanium naturally reacts with nitrogen and oxygen at room temperature [39, 40]. To avoid oxidation of the titanium layer, successive sputter depositions of 400 nm of titanium and 40 nm of titanium nitride is performed in the same tool *i.e.* without breaking the vacuum. A substrate of 220 µm is used to obtain larger curvature values, while staying in the small deformation range. A sample made only of the titanium nitride layer is fabricated and the pure titanium curvature values are calculated using the superposition principle.

Nickel vanadium

For verification purpose, a 75 nm thick nickel vanadium layer with the as-manufactured vanadium content is sputtered on a 220 µm thick silicon wafer. The content of vanadium is unknown by the author. The objective here is to evaluate whether the layer behaves elastically in the tested temperature range.

2.2 Constitutive model

Shen *et al.* [41] have shown that continuum models are valid to represent the thin film behavior, even for film thicknesses below 1 µm. They have shown that an elastoplastic analysis of the unpassivated aluminum film yields correct trends, especially if the temperature dependence of the yield stress is considered. In metal films, plasticity with Bauschinger-like phenomena is often observed. Stabilization of the thermo-mechanical response is observed after a given number of cycles. To obtain stabilization in cyclic plasticity, the saturation of the yield surface expansion is required. In this work, a non-linear kinematic hardening model according to Chaboche is chosen.

2.2.1 Chaboche model

The model from Lemaitre and Chaboche offers the possibility to integrate isotropic and kinematic hardening as well as time dependency. It allows the modeling of the Bauschinger effect, often encountered in metals. Its flexibility makes it interesting to be applied to many materials. Creep is a thermally activated phenomena, which is negligible if the working temperature stays below half of the homologous temperature of the considered material. Thus rate-independent plasticity is valid for material deformed at low temperature and modest strain rate ($\dot{\varepsilon} = 0.01\,\mathrm{s}^{-1}$ to $10\,\mathrm{s}^{-1}$). Here a rate-independent kinematic hardening Chaboche model is chosen.

The equations governing the rate independent plastic response of a material point are given

by [42]:

$$\begin{cases} f = J(\boldsymbol{\sigma} - \boldsymbol{X}) - k \leq 0, \\ \boldsymbol{X} = \sum_{i=1}^{n} \boldsymbol{X_i}, \\ \mathrm{d}\boldsymbol{X}_i = \frac{2}{3} C_i \, \mathrm{d}\boldsymbol{\varepsilon}_p - \gamma_i \boldsymbol{X}_i \, \mathrm{d}p + \frac{1}{C_i} \frac{\partial C_i}{\partial T} \boldsymbol{X}_i \mathrm{d}T \end{cases} \tag{2.12}$$

where bold letters represent tensors, $\boldsymbol{X}$ is the backstress tensor, k the yield stress, T the temperature, $\boldsymbol{\varepsilon}_p$ the plastic strain tensor, p the accumulated equivalent plastic strain, C_i and γ_i are temperature-dependent material parameters. The latter introduces the non-linearity. The rate of change of γ_i with respect to temperature is not accounted for in the evolution law of $\boldsymbol{X}_i$. Consequently, if γ_i vary with temperature, the material response predicted by the model will be temperature history dependent. However, temperature-history dependent behavior can be obtained by the use of a constant γ_i [43].

The yield criterion predicts whether the material responds plastically or elastically. The yield surface is defined by the yield function f (Eq. 2.12). This function depends on the Cauchy stress $\boldsymbol{\sigma}$, the backstress tensor $\boldsymbol{X}$, the yield stress k (here constant because only kinematic hardening is considered). The elastic domain is defined by the stress domain so that the yield function is negative. The Von Mises yield criterion is used:

$$J(\boldsymbol{\sigma} - \boldsymbol{X}) = \left(\frac{3}{2} (\boldsymbol{\sigma}' - \boldsymbol{X})(\boldsymbol{\sigma}' - \boldsymbol{X}) \right)^{1/2} \quad \text{with} \quad \boldsymbol{\sigma}' = \boldsymbol{\sigma} - \frac{1}{3} \mathrm{tr}(\boldsymbol{\sigma}) \boldsymbol{I} \tag{2.13}$$

where $\boldsymbol{\sigma}'$ is the deviator of $\boldsymbol{\sigma}$, $\boldsymbol{I}$ the identity matrix, tr denotes the trace of the matrix.

The superposition of several kinematic hardening models is possible thanks to the addition of various backstresses $\boldsymbol{X}_i$. The non-linear kinematic hardening rule depends on the plastic strain tensor $\boldsymbol{\varepsilon}_p$, the accumulated equivalent plastic strain scalar p and two characteristic coefficients of the material C_i and γ_i. Generally, the tensor $\boldsymbol{X}$ is assumed to be zero in the initial state [42]. Under this assumption and in the tension-compression case, C corresponds to the hardening modulus value in the initial state.

The evolution equation can be analytically integrated in the uniaxial case. It is given by [42]:

$$X = \nu \frac{C}{\gamma} + \left(X_0 - \nu \frac{C}{\gamma} \right) \exp[-\nu\gamma(\varepsilon_p - \varepsilon_{p0})] \tag{2.14}$$

where $\nu = \pm 1$ depends on the flow direction, ε_0 and X_0 are the plastic strain and backstress values at the beginning of each plastic flow. The stress at any time is given by $\sigma = X + \nu k$. Fig. 2.7 shows the typical stress versus plastic strain curve in tension-compression. The maximum al-

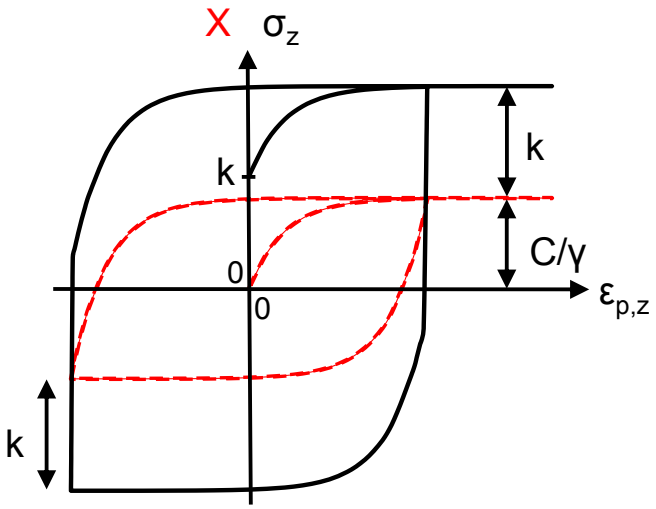


Figure 2.7: The full line shows the stress versus plastic strain in tension-compression loading. The dashed line shows the evolution of the backstress.

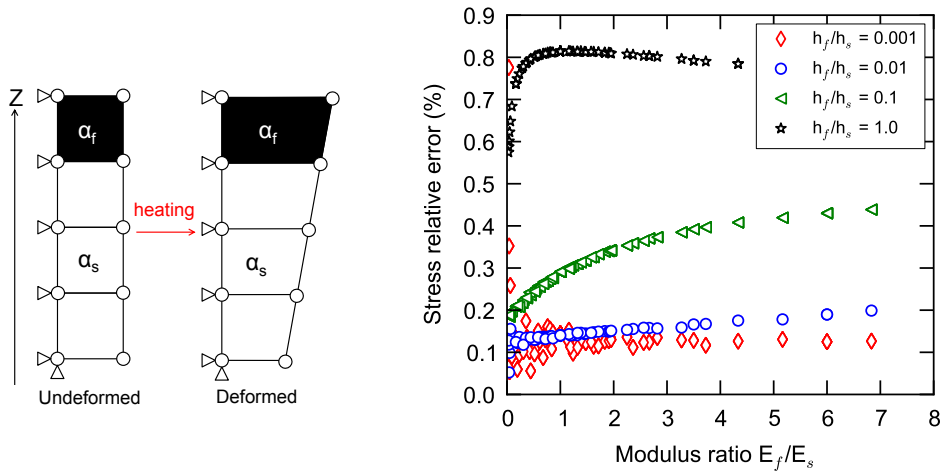
lowable stress in the material is $k + C/\gamma$. The hardening modulus behavior depends on the initial hardening modulus, the recovery parameter and the backstress.

2.2.2 Parameter identification procedure

Simulation model

A two-dimensional model, shown in Fig. 2.8a, emulates the experimental setup. The same assumptions are used as in Stoney's derivation. The simulation model requires only a single column of elements in the thickness direction (z-axis). Generalized plane strain conditions account for the symmetry in the in-plane dimension (x, y). Symmetry boundary conditions are applied on the left node set. The origin node displacement is constrained in both x- and z-direction to prevent any rigid body motion. Kinematic constraints through slider elements ensure that symmetry is also maintained on the right node set after deformation. A slider element constrains a set of three nodes by defining a slave node, which is to stay aligned with two master nodes.

In order to validate the model, we have performed a parametric study of a bilayer stack with fully elastic behavior and varying film and substrate thickness. The stress is uniform in the film layer as expected. The stress obtained from simulation is compared to the analytical solution given by Hsueh [36], valid for any film/substrate thickness ratio. The results are presented in Fig. 2.8b. For unit film-substrate thickness ratio h_f/h_s, the relative error is independent of the absolute film and substrate thickness. For thickness ratios less than one, the relative error



(a) **(b)**

Figure 2.8: (a) Two-dimensional simulation model. A single column of element features the sample layers. (b) Relative stress error between simulation and analytical solution by Hsueh [36] versus film-substrate Young's modulus ratio E_f/E_s. The lines are parameterized by the film-substrate thickness ratio h_f/h_s.

increases with increasing film-substrate modulus ratio E_f/E_s. For a given set of properties for substrate and film, the maximum relative error is below 1 %. The simulation model gives good agreement with the analytical solution for the case of elastic material. The same simulation model is used to extract the plastic behavior.

Procedure

The goal of the mechanical testing is to provide isothermal stress versus strain curves. From curvature measurement, non-isothermal stress versus temperature curves are obtained. From the experimental data and the chosen model, approximation methods are developed to find the model parameters providing the best fit for the experimental data. In this work, the curvature measurement technique provides data for the average film stress evolution versus temperature, without an actual measurement of the plastic strain. It is clear that the temperature is linked to the strain, however the exact plastic strain induced by a given temperature is unknown. Here temperature-dependent parameters are searched. The number of parameters is large, thus it has been decided to use the Monte Carlo simulation method to solve the problem.

Material model parameters for various film thicknesses are obtained by solving the inverse problem. Assuming a material model and a set of material parameters, the thermomechanical behavior is determined by finite element simulations. Parameter values are randomly gener-

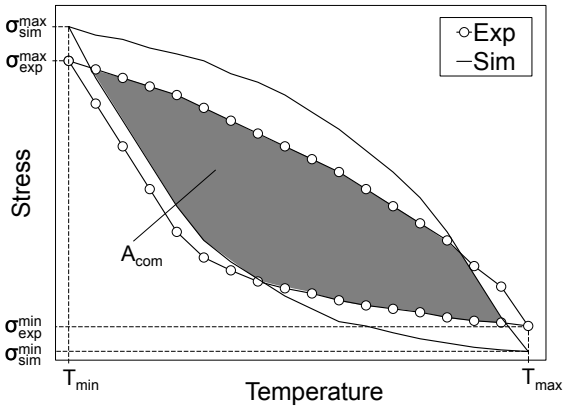


Figure 2.9: Comparison criteria for Monte Carlo simulations

ated from a uniform distribution. The bounding values are selected based on additional information on the material. In order to obtain a temperature dependent behavior, each parameter is drawn at 5 different temperatures. Yield stress and initial hardening modulus decrease with temperature. To incorporate this knowledge in the drawing procedure of one parameter set, the corresponding bound of the uniform distribution is updated to reduce the range. For instance, if the parameter k is drawn first at a temperature T_1, such that $T_1 < T_2$, for drawing the parameter at the temperature T_2 the upper bound of the distribution takes the drawn value $k(T_1)$. The simulated stress versus temperature curve is compared to the experimental data and the quality of the fit is estimated based on three criteria shown in Fig. 2.9. The stress values at the minimum and maximum temperatures of the thermal cycle are to be within ± 5 % of the experimental values, normalized by the full stress range. The common area A_{com} of the experimental and simulated curve has to be maximized and a relative difference of 15 % is accepted. The hysteresis loop area is indirectly related to the energy dissipated during the cycle, thus making it an important parameter for evaluating the fit quality. Parameter sets are repeatedly drawn and evaluated with respect to the acceptance criteria. At the end of a simulation run, a histogram reporting the counts of the accepted values for each parameter is obtained and the parameter value with the highest number of counts is used. Fig. 2.9 shows the acceptance criteria, given by:

$$
\begin{aligned}
E_{area} &= \frac{A_{exp}-A_{com}}{A_{exp}} \leq 15\% \\
d_{min} &= \frac{|\sigma_{sim}(T_{min})-\sigma_{exp}(T_{min})|}{\sigma_{exp}^{max}-\sigma_{exp}^{min}} \leq 5\% \\
d_{max} &= \frac{|\sigma_{sim}(T_{max})-\sigma_{exp}(T_{max})|}{\sigma_{exp}^{max}-\sigma_{exp}^{min}} \leq 5\%
\end{aligned}
$$

where σ_{sim} and σ_{exp} are the stress function obtained respectively from simulation and from experiment, A_{sim} and A_{exp} are the area in the hysteresis loop of, respectively, the simulated and the experimental $\sigma - T$ curve.

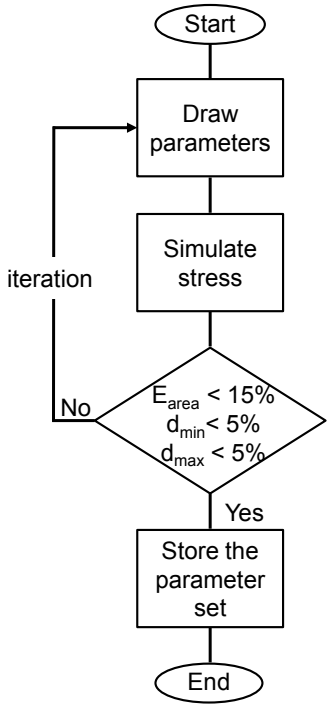


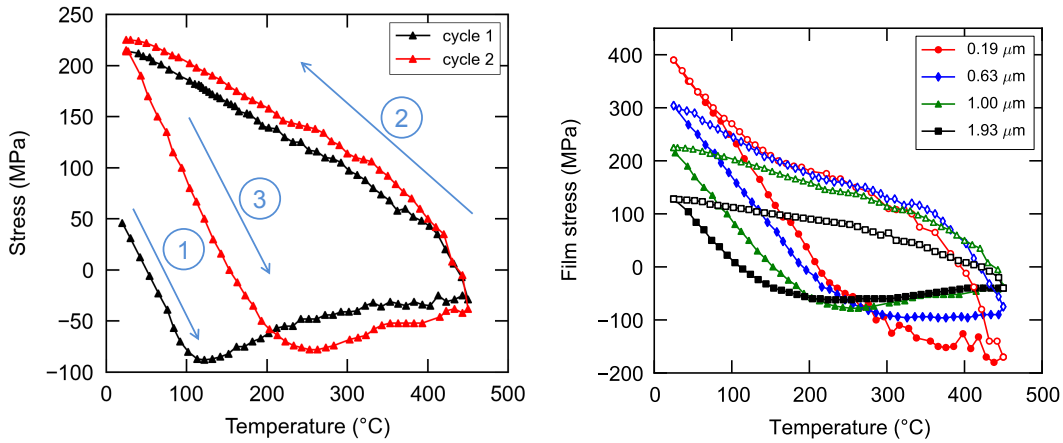
Figure 2.10: Procedure of the Monte Carlo simulations

2.3 Results and discussion

2.3.1 Aluminum

Fig. 2.11a, reproduced from [37], shows the stress versus temperature evolution for a 1 µm-thick aluminum film. At room temperature, the film is under tension, resulting from the film deposition conditions. During the first cycle, the stress becomes compressive because the thermal expansion of the film is larger than the one of the substrate. Upon further heating, the film stress reaches a minimum at about 125 °C. It then increases with increasing temperature until temperature reversal at 450 °C. The stress relaxation observed during the first cycle in the temperature range of 125 °C to 450 °C is partially explained by grain boundary volume reduction [33]. The first heating cycle cannot be used to infer the elastoplastic behavior of the film as structural changes such as grain growth occur. The aluminum stress-temperature curve has been observed to stabilize after two cycles. Thus, the stress-temperature curve for the second cycle (Fig. 2.11a) is dominated by the effects of elastic and plastic deformation. It is used to determine the elastoplastic behavior of aluminum. During the second cycle, the stress decreases linearly with temperature, with a slope given by $d\sigma_f/dT = M_f(\alpha_s - \alpha_f)$. From 200 °C to 450 °C, the film stress deviates from the linear trend. It means that the film starts to behave plastically. Upon temperature reversal at 450 °C, the film stress initially increases linearly with decreas-

ing temperature until very soon plasticity occurs. The stress measured in the region where the stress deviates from the linear behavior versus temperature is the biaxial flow stress of the film.



(a) **(b)**

Figure 2.11: Aluminum thermomechanical behavior (a) The first two temperature cycles for a 1 µm-thick aluminum film are depicted. (b) The stabilized cycles for various aluminum thicknesses. Data extracted from [37].

Fig. 2.11b shows the stabilized stress-temperature curves for various aluminum thicknesses, as reported by [37]. The thinner the film is, the higher the temperature at which plastic deformation begins. The compressive flow stress reaches a plateau at high temperature except for the thinnest film. The compressive flow strength increases from about 40 MPa to 100 MPa when the film thickness decreases from 1.93 µm to 0.63 µm at high temperature. Similarly, the tensile flow strength increases with decreasing film thickness from 125 MPa to 390 MPa for a film thickness decreasing from 1.93 µm to 0.63 µm at room temperature. It has been observed by many researchers that the flow stress of thin polycrystalline films is inversely proportional to the film thickness and reaches a plateau for the thinner films [44, 45]. Large flow stress in thin film results from the coupling of the grain size and film thickness effects [46]. A small film thickness leads to a more preponderant role of the interfaces in the material behavior. A small grain size leads to impinged dislocation motion and reduced dislocation source density.

Elastic behavior

Tab. 2.2 reports the temperature dependent elastic behavior of silicon and aluminum. The temperature dependence of the Young's modulus E_{Al} of aluminum is calculated from the experimental data by using the temperature dependent Coefficient of Thermal Expansion (CTE) reported in Tab. 2.2 and constant Poisson ratio 0.33. Tab. 2.3 reports the temperature coefficients and the Young's modulus values for the various aluminum thicknesses. The temperature

Table 2.2: The temperature dependent properties of silicon and the coefficient of thermal expansion of aluminum are provided by the literature. A constant Poisson ratio is assumed for aluminum. A linear temperature dependence is assumed for the Young's modulus E_{Al} of aluminum and the coefficients are obtained by fitting of the experimental data. E_{T_0} is the Young's modulus at the temperature T_0 in GPa, b is the temperature coefficient in K^{-1}, T in °C.

Parameter	Law
E_{Si} (GPa) [31]	$129.6 \times \left[1 - 60 \times 10^{-6}(T-25)\right]$
α_{Si} (10^6 °C^{-1}) [14]	$3.084 + 0.00196T$
ν_{Si}	0.28
α_{Al} (10^6 °C^{-1}) [14]	$23.64 + 8.328 \times 10^{-3}(T-27) + 2.481 \times 10^{-5}(T-27)^2$
E_{Al} (GPa)	$E_{Al} = E_{T_0} \times \left[1 - b(T-T_0)\right]$
ν_{Al}	0.33

coefficient of the Young's modulus is found to be $585 \times 10^{-6}\,K^{-1}$ for the various thicknesses. It is larger than the value reported for bulk, b = $480 \times 10^{-6}\,K^{-1}$ [47]. The Young's modulus at 25 °C varies from 47 GPa to 69 GPa, when the film thickness decreases from 1.93 µm to 0.19 µm. The modulus of an aluminum crystal varies from 63.2 GPa to 75.5 GPa when its orientation changes from ⟨100⟩ to ⟨111⟩ [14]. The obtained values at 25 °C are lower than the Young's modulus for the ⟨111⟩ direction, which can be explained by the polycrystalline nature of the film. The Young's modulus for the thicker film is calculated to be 26 % lower than the ⟨100⟩ Young's modulus for bulk. It can be attributed to the presence of defects such as microcracks [48]. The Young's modulus is found to be thickness-dependent.

Table 2.3: Aluminum fitted Young's modulus E_{Al}(T= 25 °C) at 25 °C. The fitted values are systematically smaller than the ⟨111⟩ value for bulk.

Thickness (µm)	Temperature coefficient b (K^{-1})	Young's modulus E_{Al}(GPa)
1.93	585×10^{-6}	47
1.00	585×10^{-6}	57
0.63	585×10^{-6}	59
0.19	585×10^{-6}	68
bulk	480×10^{-6}	63.2 to 75.5

It has been found by Fang *et al.* [49] that the CTE is thickness-dependent. They have observed the dependence of CTE on thickness, changing from $18.23 \times 10^{-6}\,K^{-1}$ to $29.97 \times 10^{-6}\,K^{-1}$ when the film thickness increases from 0.3 µm to 1.7 µm. According to their findings, the thin film CTE does not converge toward the bulk CTE, indicating an additional influence. The authors suggest that the presence of defects in the film is responsible for the CTE variation. As it is difficult to evaluate the defect density, the influence of thickness on CTE variation is not considered in this study.

Plastic behavior

The experimental data are fitted using a temperature-dependent Chaboche model with a single backstress. The obtained fit for each thickness is reported in Fig. 2.12. The simulated slopes of the elastic part of the heating and cooling paths must agree well with the experimental data, as the elastic modulus was one of the fit parameters. For the thicker film, shown in Fig. 2.12a, the heating path is well reproduced. The extent of the elastic domain upon temperature reversal is overestimated. For both 1 µm and 0.63 µm-thick films, reported in Fig. 2.12b and Fig. 2.12c the overall behavior is reproduced. However, the behavior of the film at high temperature and the exact departure points from the elastic behavior on the cooling path are only approximately agreeing with the experiments. For the thinner films, the film stress increases continuously in absolute value on the heating path while the simulation shows a non-monotonic change of the stress. Moreover, the stress behavior observed during cooling at low temperature is not well reproduced. The reason is the temperature sampling used here. Only four temperatures are taken over the total temperature interval. This choice has been made in order to limit the number of unknown parameters to be determined.

Fig. 2.13 shows the temperature dependence of the initial yield stress, the initial hardening modulus and the recovery parameter. Initial hardening modulus and recovery parameter depend linearly on temperature. The exact dependence is reported in Tab. 2.4. The initial yield stress decreases slowly with increasing temperature and exhibits a steeper decrease at higher temperature. The thinnest film has the largest initial yield stress over the full temperature range, which is coherent with previous observations. The parameters of the Chaboche model are thickness-dependent. The thickness dependence of the yield stress is expected from literature. The yield stress decreases with increasing temperature and increasing thickness. The increased yield stress for thinner films is usually explained by the combined effects of the grain size and the film thickness [46, 50].

Table 2.4: Temperature dependence of the initial hardening modulus C and the recovery parameter γ for various aluminum thicknesses, reported as $C(T) = C_0 + aT$ and $\gamma(T) = \gamma_0 + dT$.

Thickness (µm)	C_0 (MPa)	a (MPa °C^{-1})	γ_0 (-)	d (°C^{-1})
1.93	7054	-12	85	0.2136
1.00	12468	-20	83	0.1840
0.63	21317	-31	87	0.1456
0.19	30851	-55	86	0.1462

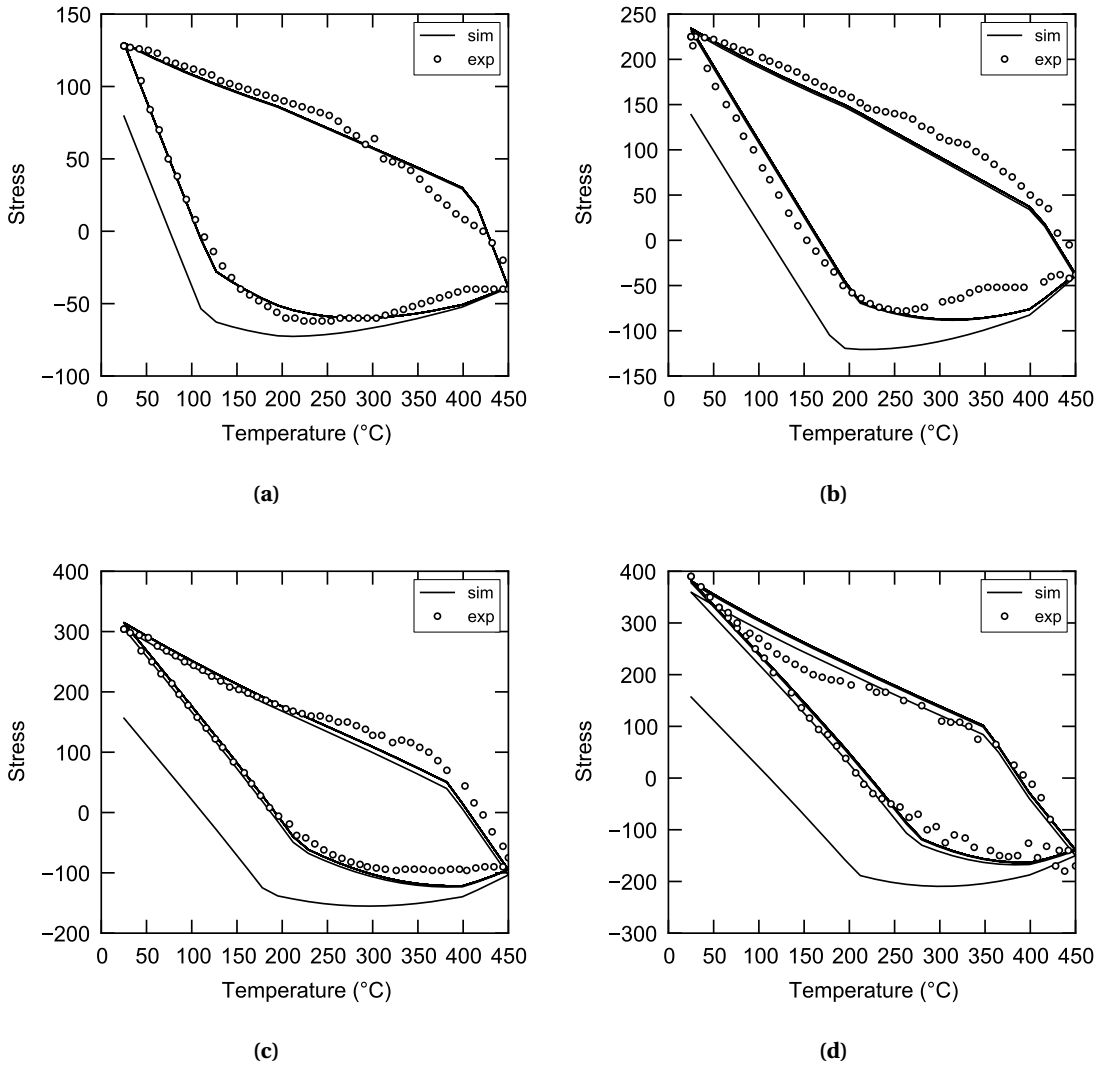


Figure 2.12: Simulated and experimental stress-temperature curves for (a) 1.93 (b) 1.00 (c) 0.63 and (d) 0.19 µm-thick aluminum films.

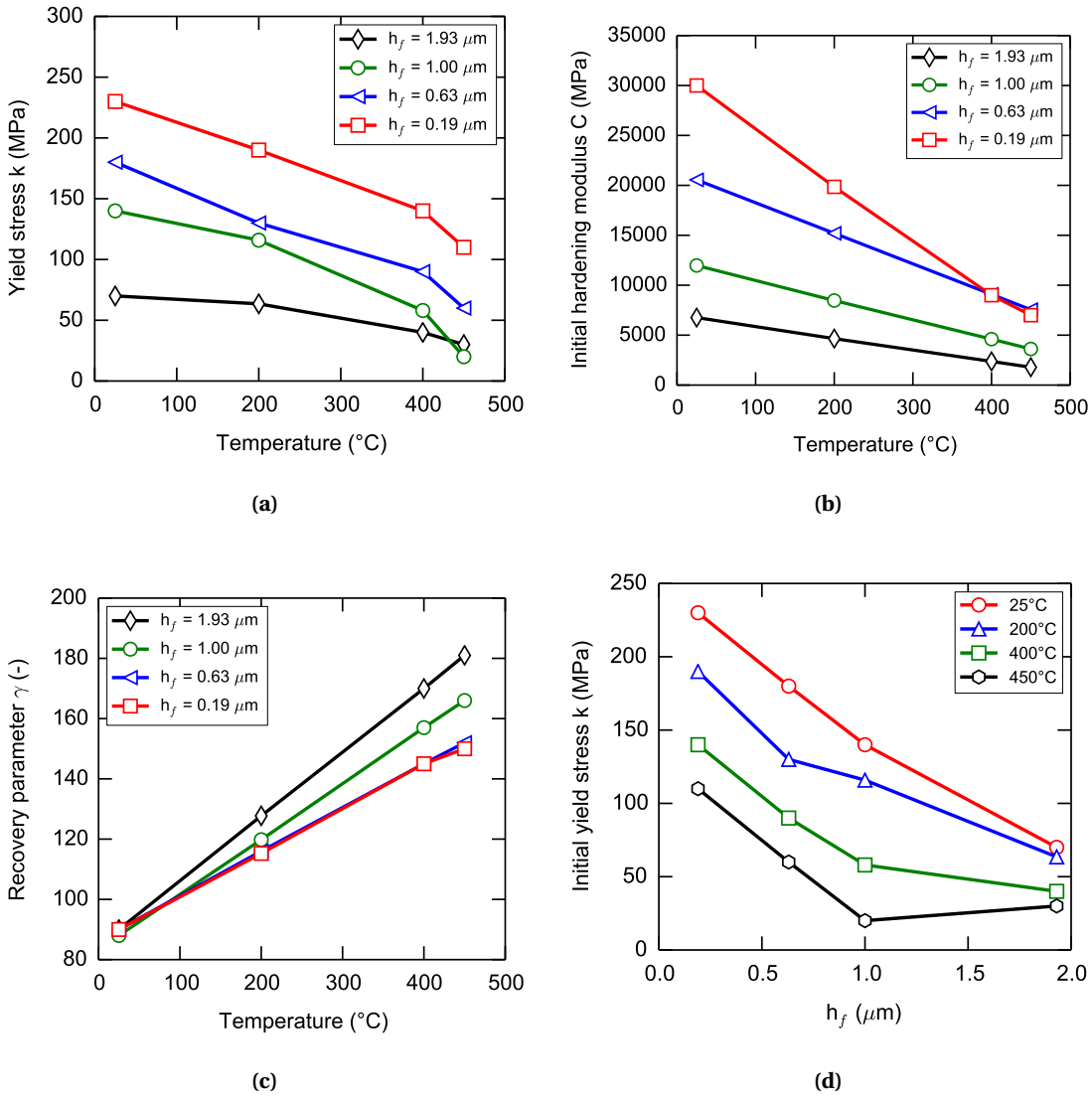


Figure 2.13: (a), (b), (c) Fitted Chaboche model parameters with a single backstress for various aluminum thicknesses. (d) Yield stress evolution versus film thickness. The curves are parameterized by temperature.

2.3.2 Solder

Fig. 2.14a shows the measured behavior of the $Au_2Cu_6Sn_2$. The first cycle, during which occurs the major part of the diffusion reaction, clearly shows a different behavior than the next cycles. Stress relaxation occurs due to phase transformation. The following cycles have a stabilized hysteresis loop around the fifth cycle. While reaching stabilization, there is relaxation of the room temperature stress. The solder layer shows limited plastic work on the range 25 °C to 450 °C. It deforms essentially elastically up to 200 °C. Upon temperature reversal at 450 °C, it does not display an elastic domain anymore.

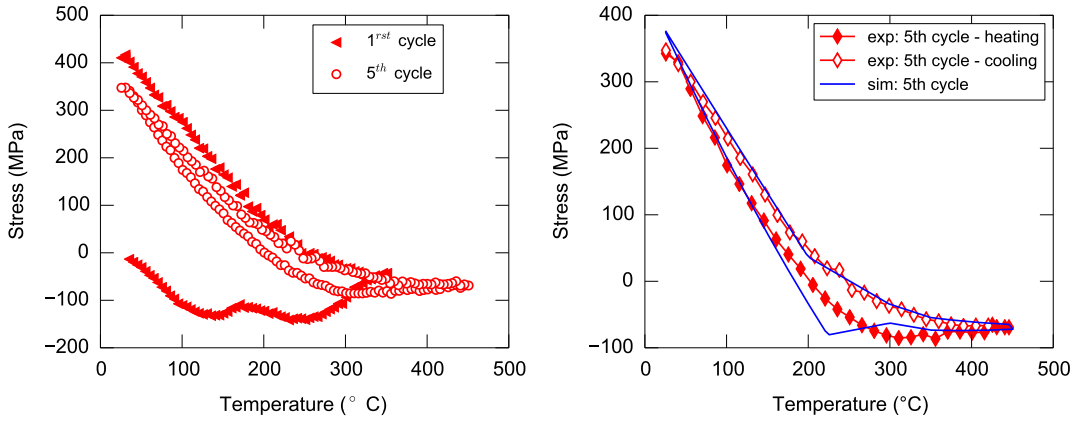


Figure 2.14: (a) Stress-temperature curve for the first and stabilized cycle for $Au_2Cu_6Sn_2$. (b) Stabilized experimental and simulated stress-temperature curves.

Elastic behavior

Fill [51] measured the thermal strain of a $Au_2Cu_6Sn_2$ sample over a temperature range from 25 °C to 250 °C. The coefficient of thermal expansion is reported to be $15.8 \times 10^{-6}\,K^{-1} \pm 1.3\,K^{-1}$ [51]. Considering the following thermal expansion coefficients for gold ($14.52 \times 10^{-6}\,K^{-1}$) [14], copper ($16.85 \times 10^{-6}\,K^{-1}$) [14] and tin ($15.0 \times 10^{-6}\,K^{-1}$) [52] and taking their weighted average $\alpha_{Au_2Cu_6Sn_2} = 0.2\alpha_{Au} + 0.6\alpha_{Cu} + 0.2\alpha_{Sn}$ results in a value of $15.96 \times 10^{-6}\,K^{-1}$ as an estimate. Considering that the layer deforms elastically up to 200 °C and assuming a typical value of the Poisson ratio for metal ($\nu = 0.3$), a Young's modulus of 135 GPa is found. The Young's modulus calculated from the experimental data slope is compared to the values obtained by weighted average of the components modulus (Tab. 2.5). From the atomic percent weighted average, a value 30 GPa smaller is calculated. Here, further mechanical testing is required to better estimate the layer elastic properties.

Table 2.5: Young's modulus of the single metal phase and of the ternary phase.

Material	Young's modulus (GPa)
Au	78.0
Sn	49.9
Cu	129.8
at% weighted average	103.5
fit $Au_2Cu_6Sn_2$	135

Plastic behavior

The previously described procedure is used to identify the parameters of the Chaboche model corresponding to the solder layer. A nonlinear kinematic hardening behavior with two backstress is found to best represent the data. The fitted parameters are reported in Tab. 2.6. The yield stress is strongly temperature dependent. The value of the yield stress at 500 °C is not realistic and the model will not be used in this temperature range. The highest temperature encountered in practice in the following simulation chapters is 200 °C. Around 200 °C, the simulation curve (Fig. 2.14b) displays a relaxation behavior. It is an artifact due to the temperature dependence of the parameters.

Table 2.6: Temperature dependent parameters of the Chaboche model with two backstresses for $Au_2Cu_6Sn_2$.

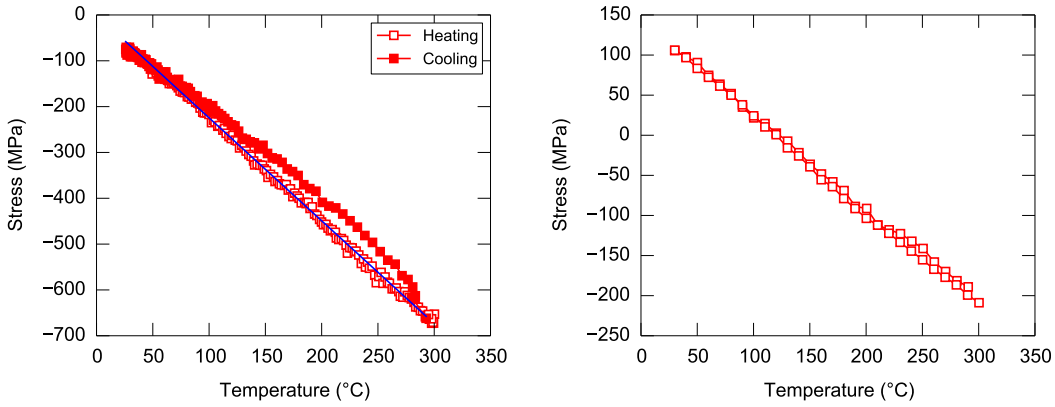
Temperature (°C)	k (MPa)	C_1 (GPa)	γ_1	C_2 (GPa)	γ_2
25	400	5.0	10	5	1
200	68	5.0	10	5	1
300	15	5.5	10	5	1
350	10	6.5	10	5	1
500	1	7.0	10	1	1

2.3.3 Titanium

Both titanium and titanium nitride are found to behave elastically when thermally cycled from 25 °C to 450 °C as shown in Fig. 2.15. Shan *et al.* [53], who tested titanium under nanoindentation, report that titanium has a very high yield strength. Here no plastic deformation is observed because the induced thermal strains are not large enough to cause plasticity.

Titanium nitride Young's modulus depends on the quantity of nitrogen. The larger the nitrogen content, the larger the Young's modulus. Torok *et al.* [54] reported that the titanium nitride Young's modulus can vary from 81 GPa to 616 GPa due to the change in nitrogen content.

In the upcoming chapters, only titanium is considered. As it is found that it behaves essentially



(a) **(b)**

Figure 2.15: Stress-temperature curves for (a) as measured titanium nitride (40 nm) and (b) titanium (400 nm) after removal of the titanium nitride contribution.

elastically in the temperature range of interest, literature properties will be used in the simulation chapters. A thermal expansion of $8.36 \times 10^{-6}\,\mathrm{K}^{-1}$ and a Young's modulus of 115 GPa and Poisson ratio of 0.33 will be used [40].

2.3.4 Nickel Vanadium

The nickel vanadium film undergoes some kind of transformation during the first temperature cycle as shown in Fig. 2.16. After three cycles, it behaves elastically. The large peak might be caused by crystallization and deformation of the film [33]. More detailed investigation of the microstructure is required to identify the mechanisms at stakes during the first cycle. The nickel vanadium film sees large temperatures during fabrication and assembly, but not anymore after soldering. Thus an elastic behavior of the layer will be assumed for simulation.

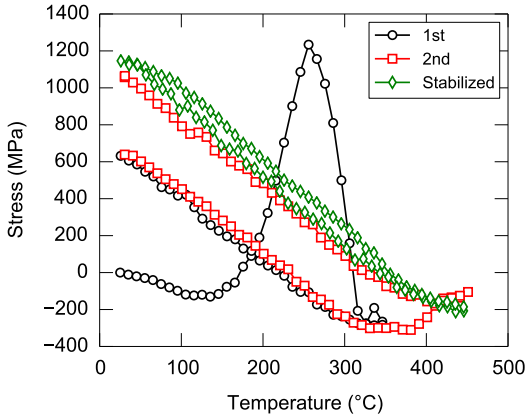


Figure 2.16: Stress-temperature curve for a nickel vanadium film.

2.3.5 Conclusion

Various metal layers, usually used in semiconductor industry as barrier or adhesion layers are found to behave essentially elastically under thermal cycling. The solder system AuSn-Cu, once reacted, behaves plastically. However, it undergoes a limited plastic work during thermal cycling.

3

Die-attach degradation assessment

THE delamination of thin films on a substrate has been intensively studied [14, 55]. Peeling, wrinkling, buckle delamination, spontaneous delamination and delamination under loading are observed [56–58]. The physical mechanisms of separation are determined by the nature of the material, but they also depend on temperature, chemical environment, loading rate and other factors, such as friction or roughness [58, 59]. Residual stresses influence significantly the delamination behavior. Generally, compressive residual stresses are beneficial to prevent delamination. Too large compressive stresses in multilayer structure might lead to bulging [60]. In case of interfacial delamination, the fracture characteristics and the mechanical properties of both materials have to be considered. In a component, delamination, voiding and film cracking are the predominant failures. In operation, such failures will lead to the formation of hot spots *i.e.* locations where the non-uniform power distribution results in very high temperatures, possibly leading to component failure either due to electrical phenomena or mechanical integrity loss. In the semiconductor industry, reliability of the devices is investigated by means of accelerated tests. These tests are established by standards and are considered as properly simulating field conditions. Here a typical reliability test, temperature cycling, is used to investigate the die-attach degradation.

In this chapter, the die-attach and backside metalization degradation is triggered using two types of temperature cycling tests for a given type of components, soldered with the previously studied solder material. Temperature cycling, as described in the standard for qualification

test, is used. As this test is time-consuming, roughly 40 min/cycle, a custom setup is developed. It allows to cycle only two devices at a time, but it performs temperature cycling 8 times faster than the standard temperature cycling test. The evolution of the degradation is monitored at regular cycle intervals by imaging the devices with SAM. This non-destructive technique allows to put the devices back in test and account for device variability as the degradation of one specific device is monitored at discrete time interval. The failure modes are identified by performing cross-section and Focused Ion Beam (FIB) cuts of the devices and imaging them using Scanning Electron Microscope (SEM). The characteristics of the degradation, such as growth rate, are reported.

3.1 Accelerated life test

3.1.1 Sample description

The Device Under Test (DUT) are Silicon Carbide (SiC) Schottky diodes packaged in TO-220, as shown in Fig. 3.1. The SiC chips are soldered with diffusion solder to improve their overall thermal dissipation capability [17]. Indeed, the diffusion solder layer is much thinner than the typically used soft solder and the diffusion solder material has a better thermal conductivity. Schottky diodes with two different current ratings are tested. For such devices, an increase in current rating means an increase of the chip area. Usually, these devices are designed such that only one wire-bond is used to link the chip to the lead. However, in case of very large current ratings, two wire-bonds might be required. The tested devices have either a rectangular shape with a small area of value 0.57 mm^2 or a square shape with a large area of value 2.5 mm^2. In order to reduce inductive effects, the wire-bond length must be minimized by placing the chip as close as possible to the lead where the connection is made. The chip has usually a backside metalization made of various barrier layers to prevent unwanted diffusion from for instance gold into the chip, which would then act as a contaminant. Buffer layers might also be implemented to mechanically decouple the leadframe from the chip. Indeed, mechanical stress in the chip leads to possible change of the electrical parameters due to the piezoresistive effect.

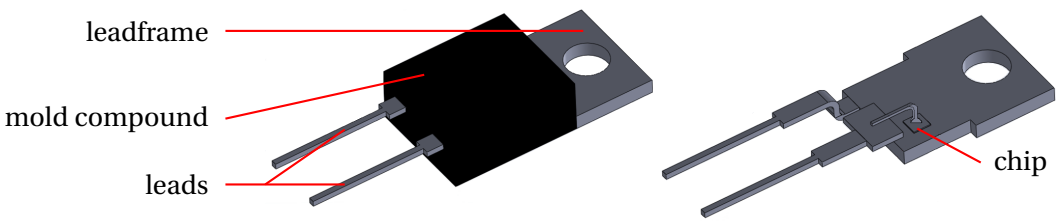


Figure 3.1: Device description

3.1.2 Temperature cycling

Temperature cycling simulates alternating temperatures during service life. It evaluates the ability of components and solder interconnects to perform their required function under alternating temperature for a given period of time. The induced mechanical stresses can result in permanent electrical and physical changes. The specific test conditions depend on the application. Standards, such as AEC-Q101, describe the minimal stress test qualification for one device type depending on the application. Specific applications might require more demanding qualification. For instance, stress test qualification for discrete semiconductor devices, as defined by AEC-Q101, requires that 77 samples withstand 1000 temperature cycles between −55 °C to 150 °C with zero fails. Failure criteria are mainly defined by electrical parameter drift. The test conditions do not represent exact field conditions. Test temperatures are usually higher than actual field temperatures to accelerate degradation. However, exaggerated acceleration may induce failure mechanisms usually not encountered in the field.

Temperature cycling is described in detail in the JEDEC standard JESD22-A-104. The tests were performed in a dual-chamber tool, in which the air is permanently heated or cooled to the maximum or minimum test temperature. The DUT are placed on a moving tray that travels between the two chambers. The devices are first loaded in the upper chamber, which is then heated to the maximal temperature. Then the cycling itself, with platform traveling starts. The heating and cooling rates are not controlled in this kind of chamber. A typical temperature profile is given in Fig. 3.2. A full cycle lasts about 40 min. For a test of 1000 cycles as required by qualification, it means that the test lasts about one month. Temperature uniformity in the chamber is checked annually and online monitoring is done. The temperature in the chamber is monitored by thermocouples. Dwell times of roughly 8 min at high temperature and 10 min at low temperature are implemented.

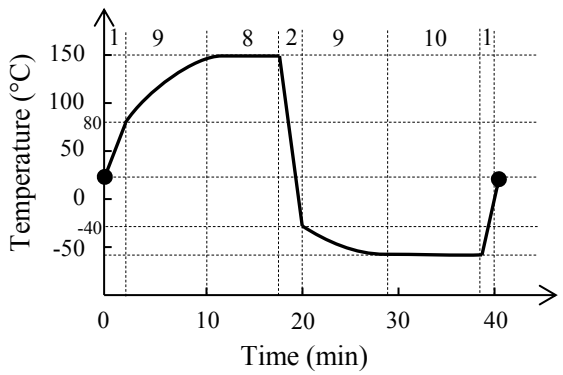


Figure 3.2: Temperature cycling temperature profile. A dwell time of 10 min is used. Heating and cooling rates are roughly 15 °C min^{-1}. A full cycle lasts 40 min.

3.1.3 Fast passive heating test

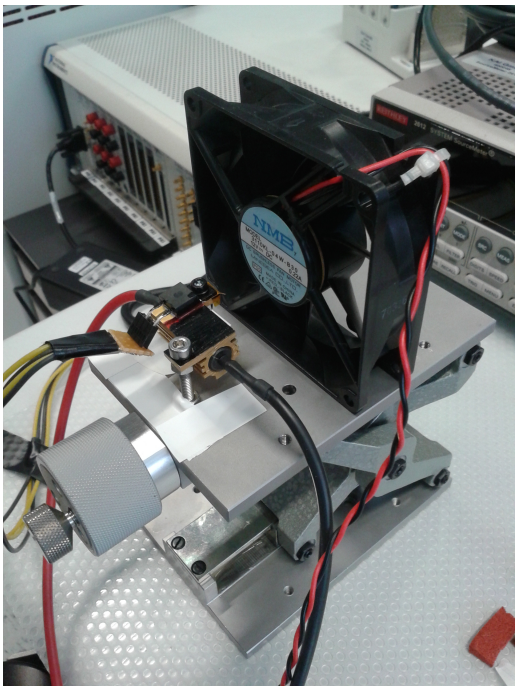
As mentioned in the previous section, standard temperature cycling is a time-consuming test. Thus a fast passive heating test bench is built to thermally stress the devices in a short period of time.

Test bench description

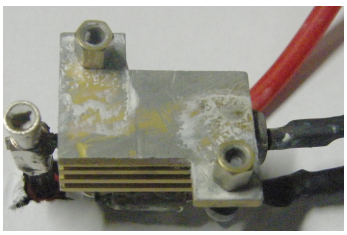
Fig. 3.3 shows photographs of the test bench developed in this work. Fig. 3.3a shows the power resistor, with a mounted diode. The fan is located close to the assembly. Heating and cooling of the DUT have to occur fast enough so that the total temperature cycle duration is in the order of a couple of minutes. The Joule effect is used for heating, that is a power resistor of resistance 4.7 Ω and a power rating of 50 W is used as heating element (see Fig. 3.3b). The resistor is powered at 15 V, which corresponds to slightly less than its maximum power rating due to cable and connection resistances. Active cooling is obtained by means of a fan. The heating and cooling elements are alternately powered by the intermediary of a C-driver, used here as an electrical switch. The C-driver logic is controlled by a signal generated by a Data Acquisition (DAQ) board, driven by a Labview routine. The temperature is monitored by measuring the voltage drop at the DUT when powered with a small current of 5 mA so as not to cause self-heating of the device. The DUT are diodes, whose forward voltage V_{AC} depends linearly on temperature. The temperature coefficient of each diode type has been measured independently under thermal air stream and is used in the Labview routine to interpret the forward voltage as temperature. As the evaluation of the temperature coefficient is time-consuming and is not performed on each single tested diode, three diodes of each type have been tested and the average temperature coefficient is used. The ambient forward voltage of each diode is measured using the Source Measurement Unit (SMU) before starting each measurement, as it varies significantly from device to device and the actual laboratory temperature varies. The SMU output is read every ms. The read value is compared against the calculated value from the user input. If it is equal or above the maximum value specified by the user, the C-driver is instructed to open the circuit of the resistor and start powering the fan. Wearing out of the custom-made connector (Fig. 3.3c) results in faulty diode readout. Thus the connector must be changed regularly. The Labview routine writes a control file containing the time and the voltage readout. Plotting of the control file allows to easily checkl if the connector is faulty.

As an example, the measurement procedure to thermally cycle a diode for 100 cycles from 50 °C to 150 °C is described here:

1. Mount the diode on the resistor, plug in the resistor, plug the specific connector on the diode for forward voltage measurement,



(a)



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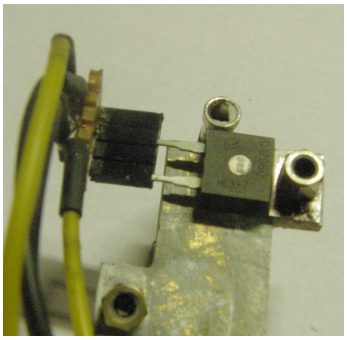


(c)

Figure 3.3: Test bench. (a) The power resistor is placed close to the fan to allow for rapid cooling. A diode is screwed onto the resistor. (b) The power resistor is shown. (c) A zoom of the diode attached to the resistor is shown. The diode is connected using the custom-made contact shown on the left. The contact degrades under thermal cycling, resulting in a faulty diode readout. As a result, the full connector must regularly be changed.

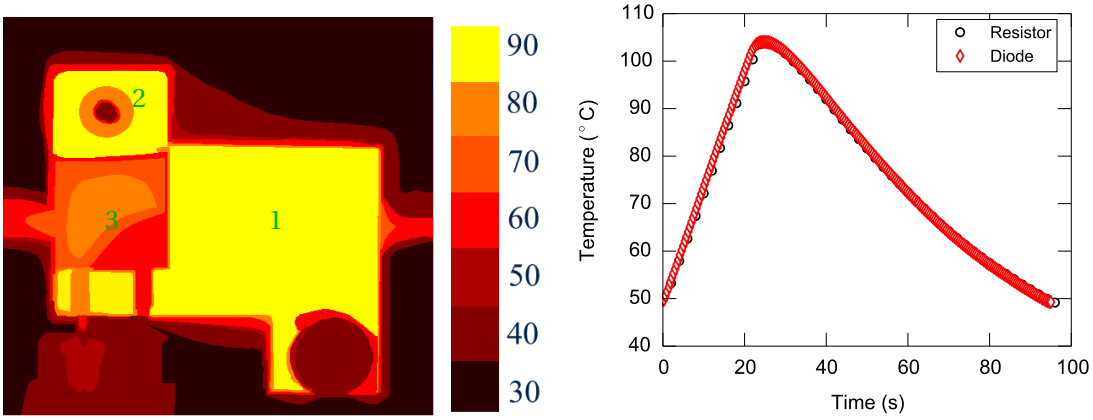
2. Turn on the voltage generator, the computer and the SMU
3. Reinitialize the C-driver using the mechanical switch,
4. Measure the diode voltage drop using the SMU and the laboratory temperature using a thermocouple,
5. Fill the Labview routine interface (voltage drop at ambient temperature, ambient temperature, minimum temperature T_{LOW}, maximum temperature T_{HIGH} and number of cycles, file name),
6. Start the measurement.

Temperature gradient evaluation

The temperature gradient induced in the package is evaluated in order to decide whether the temperature field inhomogeneity has to be considered in the subsequent simulations. To evaluate the thermal gradient induced in the device during a thermal cycle, InfraRed Thermogra-

phy (IRT) is used. In order to approximate the black body behavior as closely as possible, all the metallic surfaces are painted black. A black-painted body reaches a very high coefficient of absorption. Black surfaces and mold compound are assumed to have an emissivity of $\varepsilon = 1$. Thermal paste is used to improve the contact between the leadframe and the resistor. An infrared camera is used to constantly monitor the radiation emitted by the device and the resistor. The temperature map of the device is recorded during a temperature cycle. The available data are:

1. the temperature of the diode junction by the measurement of the forward voltage and the knowledge of the temperature coefficient;
2. the temperature of the resistor surface measured by IRT (assumed to be identical to the one of the leadframe bottom);
3. the temperature at the top of the mold compound, measured by IRT.



(a) **(b)**

Figure 3.4: (a) Temperature map of the setup at 100 °C. The resistor surface temperature (1) is identical to the temperature at the top of the exposed leadframe (2). A temperature gradient is observed at the top of the mold compound surface (3), caused by the geometry of the leadframe. (b) Diode junction temperature (forward voltage measurement) and resistor temperature (infrared measurement) for one temperature cycle from 50 °C to 100 °C. Diode junction and resistor surface temperature are identical, indicating that the materials in between have a low thermal resistance and low thermal mass. This curve corresponds to a typical temperature cycle obtained using the fast passive heating test setup.

Fig. 3.4a shows the temperature map obtained at 100 °C. The temperature is uniform and identical at the surface of the resistor and on the top of the heat sink (leadframe). The thermal gradient in the thick copper leadframe is negligible as expected from copper high thermal conductivity. The temperature on the top of the mold compound is inhomogeneous, and correlates with the leads' geometry (see Fig. 3.1). Indeed the right lead is much wider than the left one, thus improving the thermal dissipation in this part of the mold compound. The bulky

lead's presence reduces the temperature at the mold compound top surface by 20 °C at 100 °C. Except for the bottom right corner, the temperature at the top of the mold compound has a concentric distribution, as part of the heat is dissipated through the sidewalls of the package. The temperature change across the mold compound of 3.13 mm thickness is roughly 20 K: the temperature gradient is about 7 K mm^{-1}.

Fig. 3.4b shows the diode junction temperature and the heating resistor temperature versus time. The diode junction temperature is calculated from the recorded evolution of forward voltage versus time. The diode junction is usually located in the upper part of the chip. The heating resistor temperature is obtained by averaging the temperature on a 1 mm^2 area on the infrared maps. The temperatures of the resistor and the diode are matching very well, indicating that there is no temperature gradient in the stack chip, backside metalizatons, leadframe, resistor. The thermal mass of the system is dominated by the resistor, which is bulkier than the leadframe-metalization-chip stack. Thus the negligible thermal gradient indicates that the thermal contact resistance of the materials between the resistor and the upper part of the chip is negligible.

3.1.4 Differences between the tests

As already mentioned, the fast passive heating test is much faster than the temperature cycling test. However, as shown by Fig. 3.2 and Fig. 3.4b, the two types of cycling differ by the dwell time. Temperature cycling test imposes a 10 min dwell time, while no dwell time is used in the fast passive heating test. In our case, it was not possible to use the standard tool to do cycling without dwell time, which is the reason why the fast passive heating test was developed. Dwell time is believed to have a significant impact on die-attach reliability [61].

For lead solder, dwell time has a significant impact on solder degradation due to creep effects. Creep is a time-dependent deformation under a certain applied load, occurring preferentially at high temperature. It consists of various mechanisms such as bulk diffusion, grain boundary diffusion or dislocation climb. The "high" temperature is defined by comparison with the material melting point by using the homologous temperature. The homologous temperature of a material is the ratio between its operating temperature and its melting temperature, both given in absolute temperature. Usually, creep is expected when the homologous temperature exceeds 0.5 as its various mechanisms are thermally activated. Lead based solder joints are known to creep at room temperature, corresponding to a homologous temperature of 0.62. Here the studied solder material at room temperature has a homologous temperature of 0.36. Thus creep is not expected to be a significant damage mechanism. Zhuang *et al.* [61] have shown by simulation that creep strain is more significant than the other inelastic strain when considering cooling rates below 10 K min^{-1}. Here the heating and cooling rates are much larger

than $10\,\mathrm{K\,min^{-1}}$.

Another significant difference is that the fast passive heating test cycles the devices between 50 °C to 200 °C while the standard temperature cycling is between −55 °C to 150 °C. Usually the low temperature part of the cycle is believed to contribute significantly to component degradation [61]. Indeed, significant plastic strain accumulates during the cooling cycle. In addition, the strain-free temperatures of most of the materials involved in the component are their processing temperature which is around 200 °C for the mold curing. Thus negative temperature results in the largest thermal strain which in turn might lead to the worst case regarding the stress state.

Here, it appears that neither the dwell time nor the negative part of the temperature cycle are significant for the die-attach degradation, as critical delamination is observed also in the fast passive heating test. As already mentioned, the dwell time is not expected to be very critical due to the very low homologous temperature of the die-attach at room temperature. Considering the results of the previous chapter, the negative temperatures might not be too significant for the die-attach due to its limited plastic work during one thermal cycle, as we have seen that the hysteresis loop is small.

3.2 Measuring delamination

3.2.1 Scanning acoustic microscopy

Scanning Acoustic Microscopy (SAM) enables to investigate the presence of cracks and voids in materials, based on acoustic wave propagation [62, 63]. It is a non-destructive technique. All the descriptions given here apply to point focus, reflective-based C-mode SAM [64].

Working principle

The sample is immersed in an inert liquid medium, such as water, to enable acoustic wave propagation, as shown in Fig. 3.5. Using a transducer, an acoustic wave is generated, focused by means of a lens at the depth of interest and sent in the direction of the sample at normal incidence [63]. Once the wave arrives at the first interface, it is partially transmitted through the interface, depending on the medium's material properties, while the rest of the wave is reflected back to the transducer, where it is collected. The characteristics of the reflected wave, such as amplitude, polarity or time of flight are recorded for further analysis. For the inspection of a given interface, the interface depth is selected by time of flight and the reflected wave amplitude is maximized by suitable focus settings. The transducer is scanned across the sample

in several passes for image generation. Scan time varies from seconds to minutes depending on the desired resolution and the area of scan. The generated images are 255 gray levels, where black stands for low and white for high signal amplitude (air gap presence). C-mode scan focuses on a particular x-y plane at a given depth. To create this image, a time window is chosen to only allow reflection echoes from a given depth.

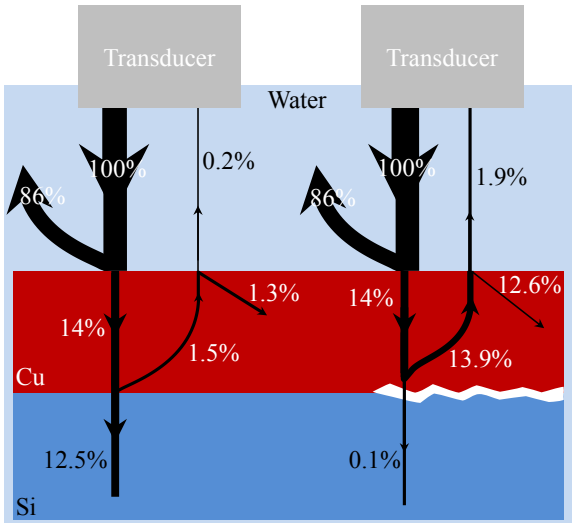


Figure 3.5: SAM working principle. The arrows correspond to the acoustic wave propagation. The left side shows a perfect interface while the right side shows a delaminated interface between chip and leadframe. The percentage of the initial wave energy that is transmitted or reflected is indicated on the arrows. Calculations are based on the specific acoustic impedance reported in Tab. 3.1.

Reflection of an acoustic signal is governed by the acoustic impedance of the involved material. Acoustic impedance defines the ability of the wave to propagate into a medium. It is denoted as z and is defined by:

$$z = \rho v \tag{3.1}$$

where ρ is the material density and v the speed of propagation of the wave in the medium. The propagation speed v depends on density and elastic properties of the medium, which in turn depend on temperature and pressure. For a wave propagating from medium 1 with impedance z_1 to medium 2 with impedance z_2 and being normally incident to the interface, the intensity reflection R and transmission T coefficients, corresponding to energy, are defined by [65]:

$$R = \left(\frac{z_2 - z_1}{z_1 + z_2}\right)^2, \quad T = \frac{4 z_1 z_2}{(z_1 + z_2)^2}, \quad T + R = 1 \tag{3.2}$$

The larger the impedance mismatch $|z_2 - z_1|$, the larger the percentage of energy that will be reflected at the interface between two media. A small acoustic impedance mismatch between the two media results in almost full transmission of the wave. The sign of the difference $z_2 - z_1$

determines the phase of the reflected wave. The waveform of the echo is inverted compared to the incident wave when $z_2 \leq z_1$. Tab. 3.1 lists acoustic impedances of the materials relevant to the application.

Resolution and related issues

When referring to SAM resolution, several points have to be considered:

- lateral resolution,
- penetration depth,
- minimum detectable air gap thickness.

SAM offers a lateral resolution mainly limited by diffraction and noise. According to the Rayleigh criterion, two objects are resolvable when their separation d is larger than a quantity determined from the focal length F of the lens, its diameter D and the considered wavelength λ. For the case of an acoustic microscope, it is reported that the theoretical minimum resolvable distance is proportional to the wavelength [62, 66]:

$$d = 1.02\frac{F\lambda}{D} \tag{3.3}$$

where d, F, λ and D are in m. Due to the experimental conditions such as a non-ideal acoustic lens and electronic noise, the theoretical maximal lateral resolution cannot be obtained experimentally, however the proportionality to λ is experimentally verified [65]. For a given lens, lateral resolution is enhanced at higher frequency [62]. The larger the wave frequency f, the smaller the penetration depth [63, 67, 68]. Indeed, when the wavelength is large compared to the grain size (here typical wavelength of 13 mm and grain of 2 µm), Rayleigh type scattering occurs and the attenuation is proportional to f^2 [62, 63]. Only very dense (metals) and thin materials can be imaged using ultra-high frequencies. An additional relevant point is the minimum size of the detected defect. In the case of microelectronics, air gaps are considered as defects. Acoustic inspection can detect very thin separations as small as 0.1 to 0.01 µm as reported by [69].

3.2.2 Image processing

Automatic measurement of the delaminated area is implemented in Labview. The full leadframe and the chip are visible in the SAM picture shown in Fig. 3.6a. The black and dark gray pixels feature the absence of voids in the layers where the ultrasound propagates while the white areas feature the presence of air gaps. The Labview routine consists of three steps:

Table 3.1: Specific acoustic impedance for materials of interest. For the thermoset, the values are approximated: the elastic modulus is estimated at 10 GPa.

Material	Density $\mathrm{kg\,m^{-3}}$	Velocity $\mathrm{m\,s^{-1}}$	Acoustic impedance $\mathrm{kg\,s^{-1}\,m^{-2}}$
Air	1.2	340	408
Water	1×10^3	1.5×10^3	1.5×10^6
Copper	9×10^3	4×10^3	40×10^6
AuCuSn	11×10^3	4×10^3	44×10^6
Silicon	2.3×10^3	8.4×10^3	20×10^6
Thermoset	1×10^3	3.1×10^3	3×10^6

1. Perform thresholding, *i.e.* digitalization of gray values to 0 and 1 values according to the average image threshold,
2. Calibrate the image scale in mm,
3. Count the pixels corresponding to the undamaged area.

The rotated and cut SAM image is shown in Fig. 3.6a. Its histogram is shown in Fig. 3.6b, where the bins are the pixel values from 0 to 255. The thresholded image is shown in Fig. 3.6c, where the red box is obtained from the particle detection routine. The mean value of the full picture histogram is used as the bound value for thresholding. All the pixels below the mean value are set to black while the rest is set to white. It means that the delaminated area and the leadframe are white after thresholding. The white particle, corresponding to the leadframe, is detected using a particle detection routine readily available in Labview. Instead of its area, the width of the leadframe is measured to reduce the error on the scale. Indeed, the edges of the leadframe are not well resolved in the image, especially the horizontal edges, while the vertical edges are well defined. Fig. 3.6d shows the zone where the black pixels are counted. The particle detection routine is then used on the "black" particle, corresponding to the undamaged chip area. Its size in pixel is recorded. The undamaged area is thus measured. Using the previously determined scale, the undamaged area is converted into square millimiter. Thus the delaminated area is calculated using the known chip size.

This method is simple but subject to error. The first error comes from the presence of bleed-outs along the chip edges. They usually appear as bright areas in pictures. For the same device, the bleed-out will appear identical over cycling. Thus its presence induces a vertical offset of the delaminated area versus number of cycle curve, but the relative changes are not affected. The second error source is the gray scale. Indeed, the range of the detected amplitude is not necessarily constant over the test, leading to a change of the gray scale convention. Deeper image processing, allowing to remove speckle noise and recalibrating the grayscale based on the wire-bond color and the leadframe color would improve the routine. However, the implemented routine already gives satisfying results.

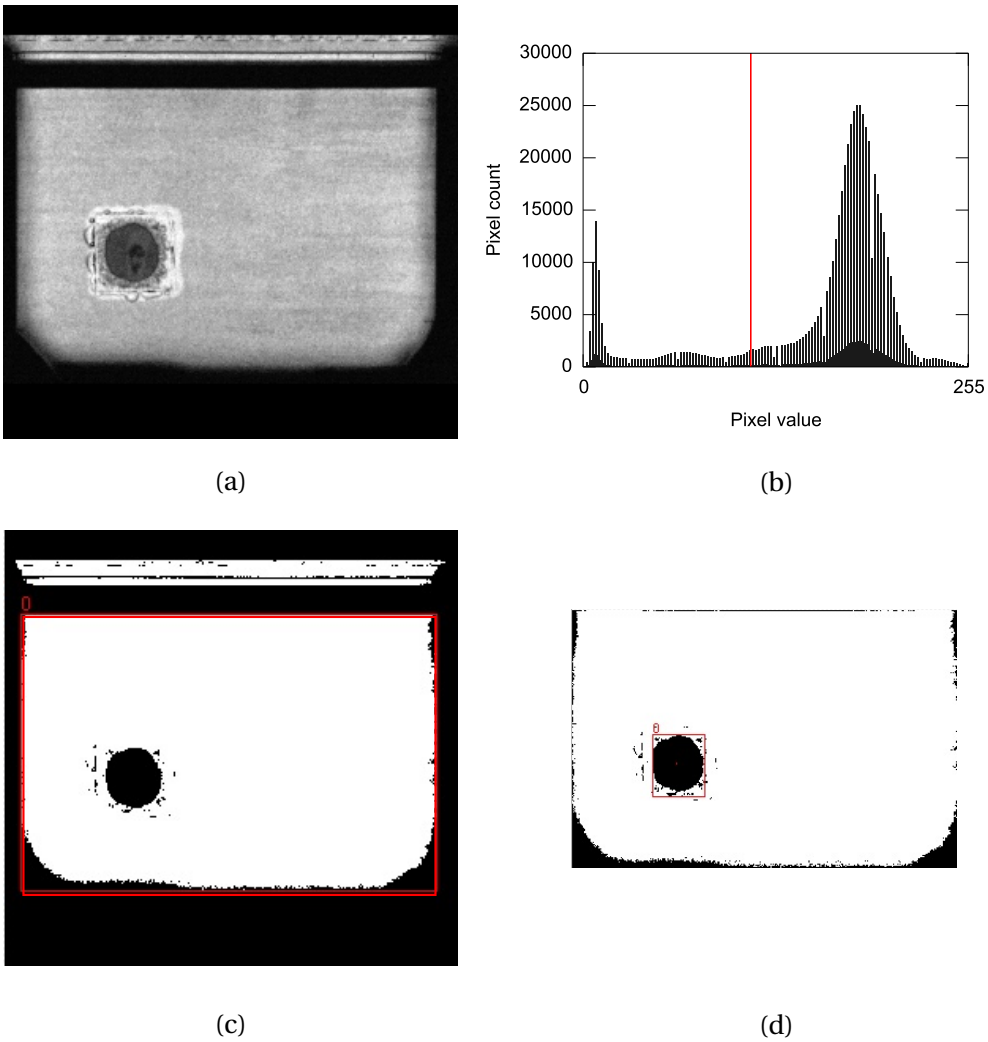


Figure 3.6: Example of the processing of SAM image. (a) Vertically rotated image. (b) Histogram of the first image. The vertical line symbolizes the threshold value of the image. (c) Thresholded image. The threshold value is the mean value of the histogram of the 255-gray level image, here 111. The particle detection routine of Labview detects the leadframe, shown as a red box in the picture. From the particle detection, the leadframe width in pixel is known. (d) Black pixel counting. The previous image is cut along the previously detected border of the leadframe. The particle detection routine is used to look for a black object.

3.3 Results

3.3.1 Failure modes

SAM pictures of devices tested under standard thermal cycling or fast passive heating indicate that air gaps are forming between the chip and leadframe. The gating of the time of flight allows to locate an interface. However, the accuracy of the localization depends on the operator. Thus it is not possible to determine the location of the forming air gaps with an accuracy of 1 µm. Consequently, the various backside metalization layers cannot be easily distinguished by gating. To locate them, cross-sectioning is performed by mechanical grinding. The grinding process locally deforms the layers, provoking material removal or displacement from layer to layer, which is harmful for subsequent observation. The obtained cross-sections are then imaged using SEM. Conclusions might be difficult to draw due to the grinding effects. Thus, FIB can also be performed on the cross-section, allowing to remove material with minimal damage to the surrounding layers. FIB is a time-consuming process so it is only performed on a small sample size, of the order of a few micrometers. The resulting FIB cut is imaged by SEM.

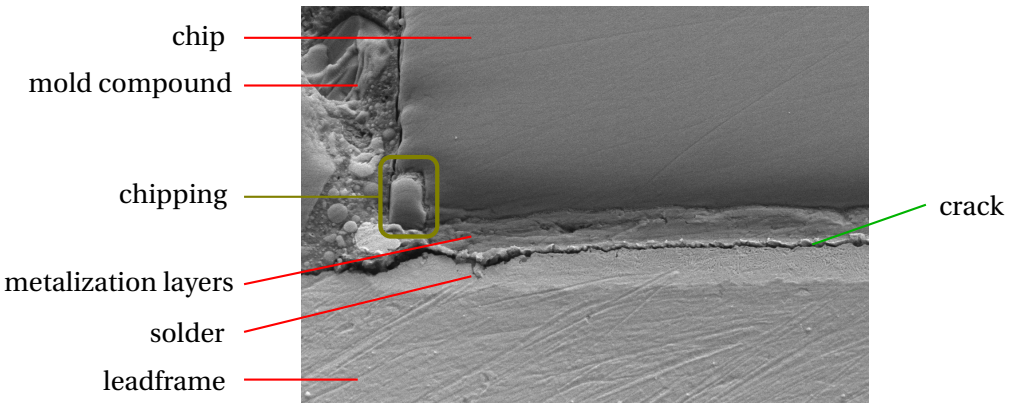


Figure 3.7: SEM micrograph of a cross-section of the package. The mold compound, chip, leadframe, backside metalization layers and solder are visible. Interfacial delamination propagates at the interface between solder and the metalization layers. The visible scratches result from grinding.

Fig. 3.7 shows a SEM micrograph of a device cross-section. The various layers can be distinguished thanks to the gray shades. The crack appears to propagate between the metalization layers and the solder layer. The mold compound is also delaminated from the leadframe. Chipping phenomena, resulting from the dicing process, are indicated. The scratches visible in the pictures result from the grinding process.

Fig. 3.8 shows a FIB cut performed on a device cross-section, perpendicular to the grinding-plane. Interfacial delamination propagates between the solder layer and the barrier layer. The

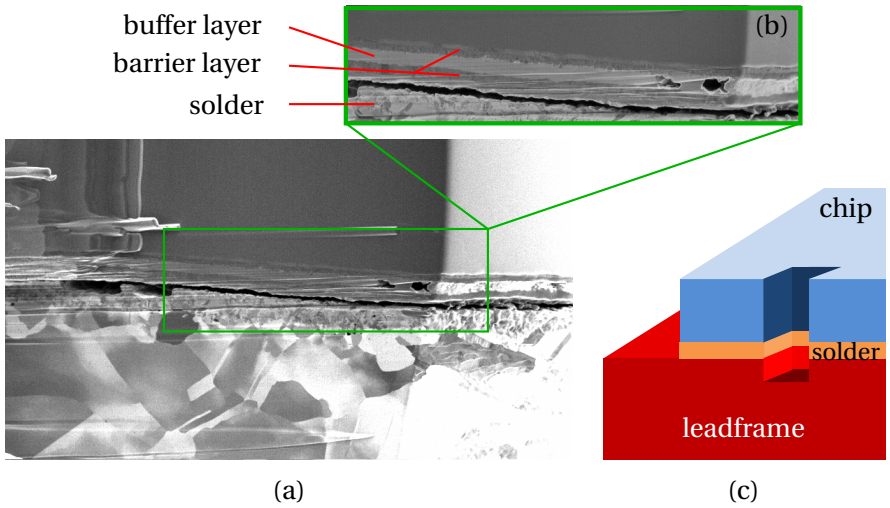


Figure 3.8: (a)SEM micrograph of a FIB cut performed perpendicular to the cross-section of the package. The mold compound, chip, leadframe, backside metalization layers and solder are visible. Interfacial delamination propagates at the interface between the solder and the metalization layers. (b) Zoom of the FIB cut. (c) Three-dimensional schematic of the FIB cut.

use of FIB allows to confirm the presence of crack, as the structure is not locally deformed by grinding but cleanly removed using inert ions.

Cracks are observed at:

- interface solder / metalization,
- in the buffer layer.

Some cracks are observed to kink, apparently from the solder / metalization interface to the buffer layer. Crack kinking from interface to the buffer layer might indicate that the solder / barrier interface is strong and so it is energetically more favorable for the crack to kink out of this interface.

3.3.2 Delamination characteristics

Delamination shape

The DUT are imaged by SAM every few cycles to monitor the evolution of the delamination of the die-attach. On the presented pictures, the darker shades of gray correspond to undamaged area, the bright areas to delaminated area. The dark spot in the middle of the chip corresponds to the wire-bond. Small solder bleed-outs are present at the chip edges. Fig. 3.9 and Fig. 3.10 show the SAM pictures for square chip devices tested under standard thermal cycling. Fig. 3.9

represents the evolution of the delaminated area for devices whose behavior is similar to the other tested devices, while Fig. 3.10 shows devices whose behavior is outside the normal observed range (see later on Fig. 3.14a). Fig. 3.11 and Fig. 3.12 show the SAM pictures of the rectangular chip tested under fast passive heating for various loading conditions and number of cycles. Fig. 3.9 and Fig. 3.11 show SAM pictures for square and rectangular chips tested either by standard temperature cycling or fast passive heating. Square chips delaminate from all edges and corners in a similar way while rectangular chips delaminate preferentially from the lower right corner in the pictures.

Fig. 3.13 shows the assumed shape of the delaminated area for the rectangular and square chip. The rectangular chip delamination is transformed into a characteristic crack length by considering a rectangular delaminated area (light gray). The measured delaminated area is divided by the chip length l_c to retrieve the corresponding crack length a. The square chip delamination is converted into crack length by considering the undamaged area A_{not} as a disk. The characteristic crack length $a_{diag} = a$ is then computed as $\left(\sqrt{2}w_c - 2r\right)/2$ where r is the radius of the undamaged area and w_c is the chip width.

Delamination evolution

Fig. 3.14a shows the evolution of the crack length versus the number of cycles for square chip devices, under standard temperature cycling. Twenty devices have been tested, imaged and returned to the test. The thick gray line corresponds to the data from the first to the third quartile. The inter-quartile range is very small. The median is indicated by the dashed line. Three devices (device 3, 15,20) are outside the thick gray line. They were identified as behaving differently judging from the observation of their SAM pictures (see Fig. 3.10). The behavior of the device 20 is observed as different because the SAM image is less bright that the corresponding normal ones, and thus not properly detected by the automated image processing routine. Device 3 and device 15 are obviously delaminating more strongly than the rest of the batch. This can be caused by the presence of contaminants on the leadframe, resulting in lower adhesion. As no detailed investigation has been performed on the two devices to confirm the reason for their deviation, these devices cannot be precluded from the subsequent analysis. The crack length a is found to be a power law of the number of cycle N:

$$a(N) = b_1 \left(\frac{N}{N_0}\right)^{b_2} \tag{3.4}$$

where a is given in mm, b_1 =0.0663 mm, b_2=0.2761, N_0 a normalization constant equal to unity. This results in a determination coefficient of R^2 = 0.92.

Fig. 3.15a shows the evolution of the crack length versus the number of cycles for rectangular

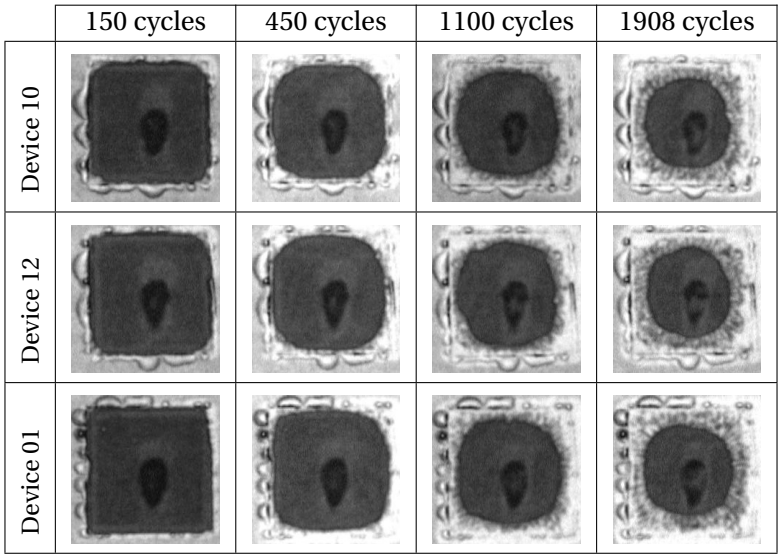


Figure 3.9: SAM pictures of the square chips for various cycles and devices. These three devices are representative of the delamination evolution. The delamination appears to start from the edges and corner leading to corner rounding. The delaminated area (bright) is roughly the same size in the three devices at the largest number of cycle.

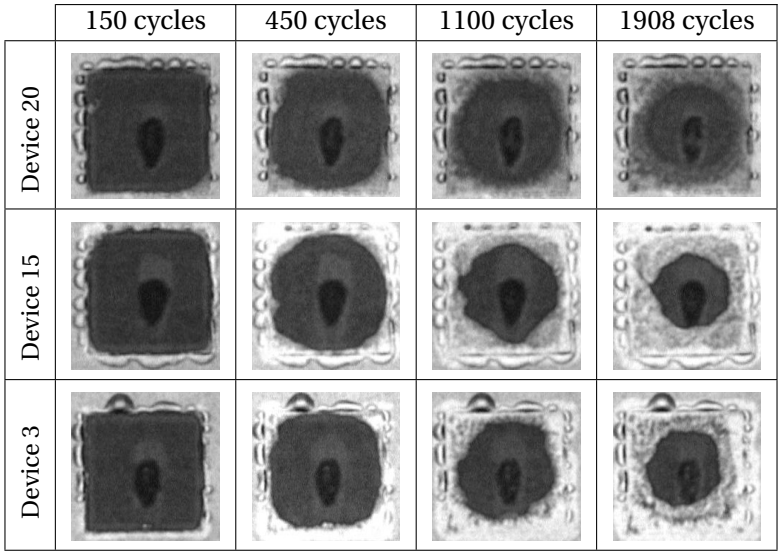


Figure 3.10: SAM pictures of the square chip for various cycles and devices. These devices are less common compared to the rest of the batch. The devices 15 and 3 are obviously delaminating more severely than the other devices (compared to Fig. 3.9) while the image for device 20 is difficult to read. Indeed the gray shades are darker than the ones in Fig. 3.9. Devices 3 and 15 might delaminate more strongly due to slightly different process conditions or local contamination. The delaminated area of device 20 cannot be analyzed properly by the automated routine. Here device variability and routine instability are demonstrated. However over a large enough number of samples, the influence is acceptable.

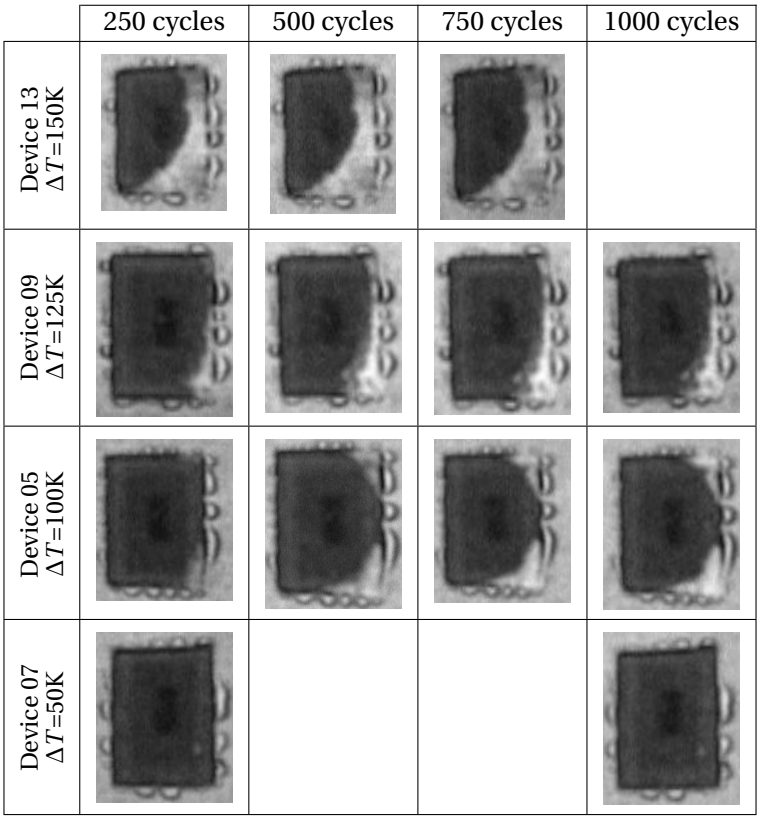


Figure 3.11: SAM pictures of the same device type (rectangular small chip) under various loading conditions and at different cycle number. These devices have been tested using the custom fast passive heating test. The smallest temperature loading does not lead to observable damage of the die-attach. The larger the applied temperature difference, the larger the resulting delamination at a given number of cycle.

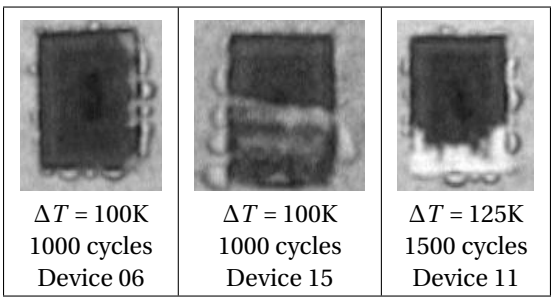


Figure 3.12: SAM pictures of the same device type (rectangular small chip) under various loading conditions. These devices correspond to circled datapoints in Fig. 3.15a.

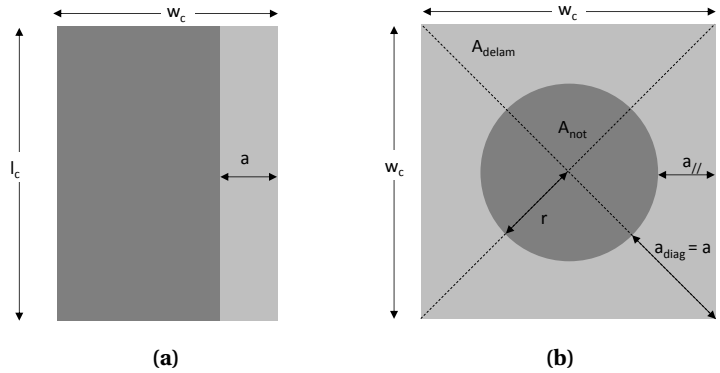


Figure 3.13: Assumed shape of the delamination (a) for a rectangular chip and (b) for a square chip. The light fray area corresponds to the presence of delamination. a corresponds to the characteristic crack length.

chip devices under fast passive heating test. In total, fifteen devices were tested under four loading conditions. The diamonds (⧫) correspond to devices cycled from 50 °C to 200 °C, the stars ($\star$) to devices cycled from 50 °C to 125 °C, the circles (•) to devices cycled from 50 °C to 150 °C and the square (■) to devices cycled from 50 °C to 100 °C. It appears that the larger temperature difference induces larger delamination for the same number of cycles. The smallest temperature difference generates no observable delamination. There exists a threshold temperature difference below which no delamination occurs in the device. It is found in the interval from 50 °C to 100 °C. Globally the larger the temperature difference, the larger the observed delamination at equal number of cycle. The circled datapoints correspond to devices that according to the SAM pictures delaminate differently (see Fig. 3.12). Device 6 does not delaminate. Device 15 shows artifacts. Device 11 delaminates from the bottom edge, while "normal" behavior is delamination starting from the bottom right corner first and then propagating to the center. The crack characteristic length versus the number of cycle is power law dependent, however the obtained coefficients of determination are below 0.5 thus the fitting parameters are not reported. The fit curves are shown in the graph.

Delamination growth rate

The delamination rate is calculated from the experimental data. As direct numerical differentiation of the data gives unstable results, a fit of the $N \rightarrow f(N)$ curve for each device is performed. The fitting function for each device is then derived and reported versus the corresponding crack length.

Fig. 3.14b shows the crack growth rate versus the crack length for the square devices, calculated as described. As no theoretical model supports the data, either a power or an exponential law

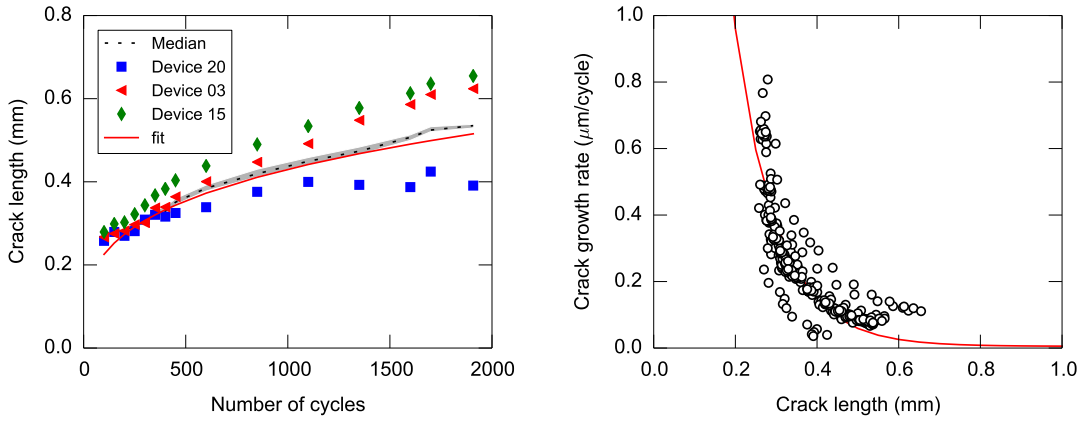


Figure 3.14: (a) Crack length versus the number of cycles for square devices tested under temperature cycling. It follows a power law of the number of cycle. (b) Crack growth rate versus crack length. A suitable power law is found for $a = f(N)$ for each device. The derivative of the model is taken and shown here, reported versus crack length.

could be used to describe it. Both approaches were tried and the exponential law appears to give a better fit. Thus the crack growth rate is described as decreasing exponentially with crack length such that:

$$\frac{da}{dN}(a) = b_1\left[1+\exp\left(-\frac{a-b_2}{b_3}\right)\right] \tag{3.5}$$

with $b_1 = 5.26\times10^{-6}$ mm/cycle, b_2 =0.741,85 mm, b_3 =0.104,17 mm. Then the determination coefficient is $R^2 = 0.78$. The crack growth rate in Eq. 3.5 is given in mm per cycle. According to this model, the crack growth rate tends toward a constant small value when the crack length becomes large. However, due to limited physical dimensions, the crack growth rate saturates and goes to zero when full delamination occurs. For better evaluation of the crack growth rate at larger crack length, more testing is required.

Fig. 3.15b shows the crack growth rate versus the crack length for the rectangular devices. The crack growth rate behaves according to a decreasing exponential law, whose parameters depend on the loading conditions. For higher temperature differences, the exponential decrease encompasses a larger range of crack sizes. For smaller temperature differences, an exponential decrease of the crack growth rate occurs already for very short crack lengths. The crack growth rate tends toward a small constant value, which, in turn, depends on the loading condition.

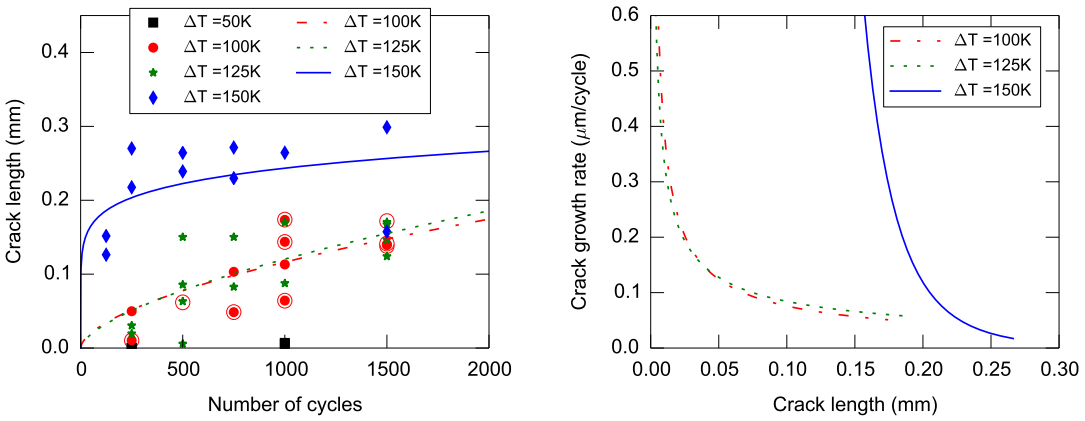


Figure 3.15: Crack evolution for rectangular chip under fast passive heating. (a) Crack length versus the number of cycles. It follows a power law of the number of cycle. (b) Crack growth rate versus crack length. A suitable power law is found for $a = f(N)$ for each device. The derivative of the model is taken and shown here, reported versus crack length.

3.3.3 Conclusions

Several failure modes are identified: interfacial delamination between solder and barrier, buffer layer cracking and crack kinking. Buffer layer cracking is delicate to study with linear elastic or elastic plastic fracture mechanics, as the layer is only a few hundreds of nanometer thin, which poses the problem of the validity of these theories. An alternative would be to use continuum damage mechanics for this failure mode. Crack kinking is a special topic, requiring detailed knowledge of the fracture energy of the involved materials. Interface delamination can be studied with an approach similar to the one used in composites, that is using energy approaches, as described in the next chapter. Additionally, this failure mode can be studied using a cohesive zone approach, which gathers all the degradations occurring at the crack front in a single damage parameter, as shown in Chapter 5. In the next chapters, only interfacial delamination between solder and barrier layer will be considered. Characteristic delamination shapes are observed using SAM. A circular delamination front is observed for square chips while a more complex shape, starting from the lower right corner is observed for rectangular chips. These shapes are believed to result from the three-dimensional stress state and thus they will not be reproducible in a two-dimensional simulation approach. The degradation is found to progress following a power law with the number of cycles. The crack growth rate behaves according to a decreasing exponential function versus the crack length. It has an asymptotic behavior toward a small constant value. These various observations will allow to qualitatively validate the simulation results of the Chapter 5.

4

Modeling interfacial delamination using fracture mechanics

In this chapter the delamination occurring at the interface between two different materials is described using a fracture mechanics approach. It consists of considering the delamination as a crack in a two-dimensional representation of the structure. Different fracture parameters exist for describing the fracture behavior, such as the energy release rate. Here it will be shown that the energy release rate describes the crack efficiently. By changing geometrical parameters and material properties, guidelines for optimizing the reliability of the structure of interest are proposed, based on the evaluation of the energy release rate.

First, an introduction to interfacial fracture mechanics with two main theories is exposed. Then the details of the strain energy release rate calculation based on forces and displacements are explained. After verifying the behavior of the finite element model, the results of the parametric study are given.

4.1 Interfacial fracture mechanics

Linear Elastic Fracture Mechanics (LEFM) deals with predicting whether an existing crack will grow further in an elastic material. A fracture criterion predicts crack growth based on fracture parameters such as stress intensity factor K or energy release rate G. Near the crack tip, under small scale yielding conditions, the stress intensity factor uniquely describes the stress field distribution. Consequently, it is often used to evaluate crack propagation. The energy release rate is linked to the stress intensity factor by the material elastic constants. Thus it is also used as a fracture parameter.

What has been explained so far applies to homogeneous elastic materials. The treatment of interfacial cracks is similar and will be explained in this section. In the case of an interfacial crack as shown in Fig. 4.1, four zones are defined at the crack tip, each described by its specific hypothesis. In the K-dominated zone, also called singularity zone, the stress intensity factor uniquely describes the stress field. In this zone, the stress field shows an inverse square root dependence on the crack tip distance. The plastic zone which develops at the crack tip in metals must be negligible compared to the K-dominated zone. Such a situation is called small scale yielding. It ensures the validity of using LEFM in metals. The oscillation and contact zones are specific to interfacial fracture mechanics. They will be explained in the next sections.

4.1.1 Small scale contact

In interfacial fracture mechanics, similar to homogeneous materials, the fracture parameters calculated from the crack tip stress field allow predicting crack growth. The crack tip stress field solution for a crack along the interface of two semi-infinite plates by Williams [70] is presented here. The situation is depicted in Fig. 4.1. The two materials behave isotropically. The upper material (material 1) and the lower material (material 2) are only defined by their shear modulus μ_i and Poisson ratio ν_i. The Cauchy stress tensor is defined using a scalar potential function Φ, called the Airy stress function [71]. The stress compatibility equation formulated in terms of the Airy stress function results in the following equation, called the biharmonic equation:

$$\nabla^2\nabla^2\Phi_j = 0, \quad j = 1,2 \tag{4.1}$$

where Φ_j represents the Airy stress function in the material j and ∇^2 is the cylindrical Laplace operator given by:

$$\nabla^2 = \frac{\partial^2}{\partial r^2} + \frac{1}{r}\frac{\partial}{\partial r} + \frac{1}{r^2}\frac{\partial^2}{\partial \theta^2}. \tag{4.2}$$

The shear stress $\sigma_{r\theta}$ and the normal stress $\sigma_{\theta\theta}$ along the crack faces ($\theta = \pm\pi$) vanish. The stress and displacements are continuous along the material interface ($\theta = 0$). The crack boundary

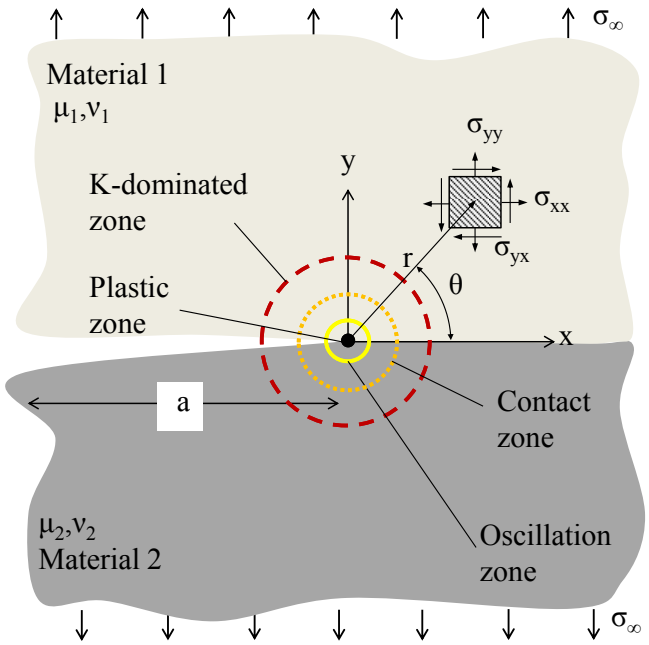


Figure 4.1: Interfacial crack between two isotropic materials with shear stress μ_i and Poisson ratio ν_i under remote tensile loading σ_∞. Four zones are depicted around the crack tip, corresponding to the successive hypothesis required to applied linear elastic fracture mechanics. The point corresponds to the plastic zone. The oscillation zone is delimited by a solid line, the contact zone by a dotted line and the K-dominated zone by a dashed line.

conditions are summarized here:

$$\begin{array}{cc} \theta = \pm\pi & \theta = 0 \\ (\sigma_{\theta\theta})_1 = 0 & (\sigma_{\theta\theta})_1 = (\sigma_{\theta\theta})_2 \\ (\sigma_{r\theta})_1 = 0 & (\sigma_{r\theta})_1 = (\sigma_{r\theta})_2 \\ (\sigma_{\theta\theta})_2 = 0 & (u_r)_1 = (u_r)_2 \\ (\sigma_{r\theta})_2 = 0 & (u_\theta)_1 = (u_\theta)_2 \end{array} \tag{4.3}$$

A general solution of the biharmonic equation (Eq. 4.1) is:

$$\Phi_j = r^{\lambda_j+1} F_j(\theta) \tag{4.4}$$

where λ_j are the eigenvalues. The eigenfunctions F_j of the partial differential equation are given by:

$$F_j(\theta) = \left(a_j \sin(\lambda_j+1)\theta + b_j \cos(\lambda_j+1)\theta + c_j \sin(\lambda_j+1)\theta + d_j \cos(\lambda_j+1)\theta\right) \tag{4.5}$$

where a_j, b_j, c_j and d_j are constants to be determined from the boundary conditions.

The stress components are written in terms of eigenfunctions in polar coordinates:

$$\begin{aligned}
(\sigma_{rr})_j &= \frac{1}{r^2}\frac{\partial^2\Phi_j}{\partial\theta^2} + \frac{1}{r}\frac{\partial\Phi_j}{\partial r} &&= r^{\lambda_j-1}\left[F_j''(\theta) + (\lambda_j+1)F_j(\theta)\right] \\
(\sigma_{\theta\theta})_j &= \frac{\partial^2\Phi_j}{\partial r^2} &&= r^{\lambda_j-1}\lambda_j(\lambda_j+1)F_j(\theta) \\
(\sigma_{r\theta})_j &= -\frac{1}{r}\frac{\partial^2\Phi_j}{\partial r\partial\theta} + \frac{1}{r^2}\frac{\partial\Phi_j}{\partial\theta} &&= -\lambda_j r^{\lambda_j-1}F_j'(\theta)
\end{aligned} \tag{4.6}$$

and the displacement components are given by:

$$\begin{aligned}
(u_\theta)_j &= \frac{1}{2\mu_j}r^{\lambda_j}\left(-F_j'(\theta) - (1+\kappa_j)[c_j\cos(\lambda_j-1)\theta - d_j\sin(\lambda_j-1)\theta]\right) \\
(u_r)_j &= \frac{1}{2\mu_j}r^{\lambda_j}\left(-(\lambda_j+1)F_j(\theta) + (1+\kappa_j)[c_j\sin(\lambda_j-1)\theta + d_j\cos(\lambda_j-1)\theta]\right)
\end{aligned} \tag{4.7}$$

where

$$\kappa_j = \begin{cases} 3-4\nu_j & \text{for plane strain} \\ \dfrac{3-\nu_j}{1+\nu_j} & \text{for plane stress} \end{cases} \tag{4.8}$$

and F_j' denotes the first derivative of the eigenfunction F_j with respect to the coordinate θ.

Replacing F_1 and F_2 by their expression (Eq. 4.5) in the boundary conditions (Eq. 4.3) leads to a linear homogeneous system of eight equations. For the boundary conditions to be independent of the distance to the crack tip r, the eigenvalues λ_1 and λ_2 must be identical according to the continuity boundary conditions. A homogeneous system of linear equations has non trivial solutions if and only if the determinant of the system equals zero. This leads to the following equation for the eigenvalue $\lambda_1 = \lambda_2 = \lambda$:

$$\cot^2(\lambda\pi) + \left[\frac{\frac{\mu_1}{\mu_2}(1+\kappa_2) - (1+\kappa_1) - 2\left(\frac{\mu_1}{\mu_2}-1\right)}{\frac{\mu_1}{\mu_2}(1+\kappa_2) + (1+\kappa_1)}\right]^2 = 0 \tag{4.9}$$

In the case of two different materials, no real solution exists as the expression is the sum of two squared terms. Thus a complex eigenvalue $\lambda = \lambda_R + i\lambda_I$ is chosen, which yields two equations and two sets of solutions. Only one set of solutions results in finite displacements at the crack tip. It is given by:

$$\lambda = \left(n - \frac{1}{2}\right) \pm i\varepsilon, \quad n = 1, 2, \ldots \tag{4.10}$$

where the oscillation index ε is a constant depending only on the material elastic constants and

is often expressed as a function of the Dundurs parameter β:

$$\varepsilon = \frac{1}{2\pi}\ln\left(\frac{1-\beta}{1+\beta}\right) \quad \text{and} \quad \beta = \frac{\mu_1(\kappa_2-1)-\mu_2(\kappa_1-1)}{\mu_1(\kappa_2+1)+\mu_2(\kappa_1+1)} \tag{4.11}$$

The eigenvalue solution has to allow the recovery of particular cases such as homogeneous material ($\varepsilon = 0$). Only the solution for $n = 1$ produces singular stresses at the crack tip for homogeneous material. The sign in Eq. 4.10 can be arbitrarily chosen as switching material 1 and material 2 inverts the sign of the oscillation index. The Airy stress function is thus expressed as:

$$\Phi_j(r,\theta) = r^{1/2+i\varepsilon}F_j(\theta) \tag{4.12}$$

resulting in stress with a dependence on $r^{-1/2+i\varepsilon}$. in other words, the stress field consists of an oscillating component in addition to the inverse square root singularity observed for homogeneous materials.

In analogy to the homogeneous material case, a unique stress intensity factor describes the crack tip field. However, due to the complex nature of the stress field, the concept of stress intensity factor has to be redefined for interfacial crack.

Following the definition given by Sun in [72], the complex stress intensity factor K is defined as $K = K_1 + iK_2$. The crack tip normal and shear stress, σ_{yy} and σ_{xy}, and the complex stress intensity factor K are linked by:

$$\left(\sigma_{yy} + i\sigma_{xy}\right)_{\theta=0} = \frac{K}{\sqrt{2\pi r}}\left(\frac{r}{2a}\right)^{i\varepsilon}\cosh(\pi\varepsilon). \tag{4.13}$$

The dependence on the crack tip distance is normalized by the crack length a. Such a definition allows to keep the same unit for the complex stress intensity factor components K_1 and K_2 as in the case of homogeneous materials. The real and imaginary parts of the stress intensity factor cannot be exactly interpreted as mode I and mode II stress intensity factors due to the oscillatory nature of the stress field.

The normal displacement oscillates near the crack tip, resulting in local crack face interpenetration. As this is not physically admissible, the oscillatory field solution is valid only if the interpenetration region is much smaller than a characteristic length such as the crack length. Using the definition of the complex stress intensity factor, the displacements near the crack tip are given by:

$$\begin{cases} \Delta u_y = u_y(r,\pi) - u_y(r,-\pi) = \dfrac{\sqrt{2r}}{4(1+4\varepsilon^2)\sqrt{\pi}}\left(\dfrac{\kappa_1+1}{\mu_1}+\dfrac{\kappa_2+1}{\mu_2}\right)(K_1H_1 - K_2H_2) \\ \Delta u_x = u_x(r,\pi) - u_x(r,-\pi) = \dfrac{\sqrt{2r}}{4(1+4\varepsilon^2)\sqrt{\pi}}\left(\dfrac{\kappa_1+1}{\mu_1}+\dfrac{\kappa_2+1}{\mu_2}\right)(K_1H_1 + K_2H_2) \end{cases} \tag{4.14}$$

where

$$H_1 = \cos\left(\varepsilon \ln \frac{r}{2a}\right) + 2\varepsilon \sin\left(\varepsilon \ln \frac{r}{2a}\right); \quad H_2 = \sin\left(\varepsilon \ln \frac{r}{2a}\right) - 2\varepsilon \cos\left(\varepsilon \ln \frac{r}{2a}\right) \tag{4.15}$$

The contact zone size r_c corresponds to the largest distance r to the crack tip for which the normal crack opening is zero. It is given by:

$$r_c = 2a \exp\left[\frac{1}{\varepsilon}\left(\tan^{-1}\left[\frac{1+2\varepsilon\tan\psi}{\tan\psi - 2\varepsilon}\right] - \pi\right)\right] \tag{4.16}$$

where the phase angle ψ is defined and calculated as:

$$\tan\psi = \frac{K_2}{K_1} = \frac{H_1 - H_2\,\Delta u_y/\Delta u_x}{H_2 + H_1\,\Delta u_y/\Delta u_x} \tag{4.17}$$

The contact zone is small if the oscillation index is small, *i.e.* if the material properties are not too different. For the small scale contact condition to be ensured, Rice recommends that the following condition is verified [73]:

$$r_c \leq 0.01a. \tag{4.18}$$

The oscillation zone corresponds to the region where the stress field changes sign. Williams [70] showed that the oscillation zone is confined to the crack tip. The stress oscillation can lead to erroneous evaluation, as under a remote tensile stress the stress state at the crack tip may be locally compressive. The oscillation zone size depends on the crack length and the oscillation parameter ε. The oscillation zone size for shear stress σ_{xy} is much smaller than the one of normal stress σ_{yy} in the case of a two-dimensional infinite medium with a center crack under applied tensile stress.

The stress intensity factors K_1 and K_2 can be calculated from the energy release rate. In interfacial fracture mechanics the components of mode I and mode II calculated for the energy release rate do not converge when reducing the crack extension Δa due to the oscillatory nature of the stress field. However, the total energy release rate G is still a valid indicator in the sense that it converges to a finite value when reducing the crack extension if the stress oscillation zone is much smaller than the assumed crack extension zone. The total energy release rate is linked to the stress intensity factors by:

$$G = \frac{1}{16}\left(\frac{\kappa_1 + 1}{\mu_1} + \frac{\kappa_2 + 1}{\mu_2}\right)(K_1^2 + K_2^2) \tag{4.19}$$

Both stress intensity factor and energy release rate concepts are valid in interfacial mechanics with the oscillatory fields.

4.1.2 Large scale contact in interfacial crack

When the contact zone size is comparable to the crack length, the small scale contact approach is not valid anymore. This typically happens when the crack is mainly loaded in mode II, *i.e.* shear-dominated loading. The crack faces are then in contact over a large region which requires a new solution for the stress and displacement fields. Here friction is assumed in the contact zone. The biharmonic equation must be solved for the new set of boundary conditions. Comninou [74] suggested that the Airy stress function should take the following form:

$$\Phi_j = r^{2-\lambda} F_j(\theta), \quad j = 1,2 \tag{4.20}$$

with the same conventions as for small scale contact. The boundary conditions ahead of the crack are identical to the ones of small scale contact, meaning there is continuity of the stresses and displacements along the interface. Along the crack faces, due to the presence of friction characterized by a coefficient μ, normal and shear stress components are coupled. The boundary conditions for contact with friction are summarized here:

$$\begin{array}{cc} \theta = \pm\pi & \theta = 0 \\ (u_\theta)_1|_{\theta=\pi} = (u_\theta)_2|_{\theta=-\pi} & (\sigma_{\theta\theta})_1 = (\sigma_{\theta\theta})_2 \\ (\sigma_{\theta\theta})_1|_{\theta=\pi} = (\sigma_{\theta\theta})_2|_{\theta=-\pi} & (\sigma_{r\theta})_1 = (\sigma_{r\theta})_2 \\ (\sigma_{r\theta})_1|_{\theta=\pi} = (\sigma_{r\theta})_2|_{\theta=-\pi} = -\mu(\sigma_{\theta\theta})_1|_{\theta=\pi} & (u_r)_1 = (u_r)_2 \\ (\sigma_{\theta\theta})_1|_{\theta=\pi} \leq 0 & (u_\theta)_1 = (u_\theta)_2 \\ (\sigma_{\theta\theta})_2|_{\theta=-\pi} \leq 0 & \end{array} \tag{4.21}$$

By replacing the stress and displacement components with an expression similar to Eq. 4.6 and Eq. 4.7 the boundary conditions lead to a homogeneous system of eight equations. A non trivial solution is obtained if the system determinant equals zero. The determinant vanishes if:

$$\sin^3(\lambda\pi)[\cos(\lambda\pi) - \mu\beta\sin(\lambda\pi)] = 0 \tag{4.22}$$

Obviously any integer value for λ is a root. However, the strain energy density is integrable, that is finite, only if $\lambda < 1$ [74]. The value $\lambda = 0$ is a root. However, as it leads to a stress state depending only on the coordinate θ it is eliminated. Therefore we solve for λ in the range $]0,1[$.Thus the equation giving the eigenvalue is reduced to:

$$\cot(\lambda\pi) = \mu\beta. \tag{4.23}$$

Note that, according to the Airy functions by Comninou, the stress field behaves according to $r^{-\lambda}$. Eq. 4.23 determines the order of the stress field singularity. It has to be solved on $]0;\pi[$. It depends on the friction coefficient and the Dundurs parameter. If either frictionless contact or homogeneous material is considered, the stress singularity decays as the inverse of the square

root of r. If $\mu\beta > 0$, the stress field behaves according to $r^{-\lambda}$ where $0 < \lambda < \frac{1}{2}$. If $\mu\beta < 0$, the stress singularity is stronger than an inverse square root, that is $\frac{1}{2} < \lambda < 1$. The case $\lambda = \frac{1}{2}$ corresponds to frictionless contact zone. Using the boundary conditions and the stress and displacement dependence on the Airy function, the near tip stress field is given by:

$$\begin{array}{ll} \text{Along the interface} & \text{Behind the crack tip} \\ \sigma_{xy}(r,0) = K_{II}(2\pi r)^{-\lambda} & \sigma_{xy}(r,\pm\pi) = K_{II}(2\pi r)^{-\lambda}\cos(\lambda\pi) \\ \sigma_{yy}(r,0) = 0 & \sigma_{yy}(r,\pm\pi) = -K_{II}\beta(2\pi r)^{-\lambda}\sin(\lambda\pi) \end{array} \tag{4.24}$$

and the relative displacement along the x-direction is given by:

$$\Delta u_x(r) = u_x(r,\pi) - u_x(r,-\pi) = \frac{\gamma K_{II}\sin(\lambda\pi)}{2(1-\lambda)(2\pi)^{\lambda}} r^{1-\lambda} \tag{4.25}$$

where

$$\gamma = \frac{(3-4\nu_1)(1-\beta)+(1+\beta)}{2\mu_1} + \frac{(3-4\nu_2)(1+\beta)+(1-\beta)}{2\mu_2}. \tag{4.26}$$

The crack tip stress field behavior is described with a unique stress intensity factor K_{II}. The friction coefficient μ and the Dundurs parameter β determine the order of the singularity. In the hypothesis of a frictionless contact, the singularity follows an inverse square root of the distance to the crack tip.

4.2 Strain energy release rate calculation

4.2.1 Energy release rate

Griffith [75] formulated the concept of energy balance for crack growth by considering the crack as a displacement from equilibrium. The crack is growing only if it reduces the potential energy of the system. The energy release rate proposed by Irwin [76] is a measure of the energy available for an increment of crack extension. It is defined as:

$$G = -\frac{\mathrm{d}\Pi}{\mathrm{d}A} \tag{4.27}$$

where Π is the potential energy supplied by the internal strain energy and the external forces and A is the area of one face of the crack. Since G is defined as the derivative of a potential, it is also called the crack driving force. G depends on the specimen geometry, the loading situation and the materials elastic properties.

Crack extension occurs when G reaches a critical value G_c, also called fracture energy. The fracture energy is a material property. For a brittle material, it corresponds to the energy required to

create two new free surfaces in the material. For metals under small scale yielding, the fracture energy corresponds to the sum of the surface energy and the energy dissipated by plasticity.

The energy approach described here is an alternative method to the stress intensity factor concept to evaluate crack growth. In this work, the energy approach will be used, as the energy release rate is directly calculated from the finite element simulations.

4.2.2 Modified crack closure method

Rybicki and Kanninen [77] explained how to calculate the energy release rate based on the consideration of the forces and displacements occurring at the crack tip in a finite element mesh. Later Raju [78] showed step by step the approach to this calculation. The method is based on the following hypothesis. If a crack extends by a small amount Δa, the energy absorbed in the process is equal to the work required to close the crack to its original length. In addition it is assumed that a crack extension of Δa does not significantly modify the stress state at the crack tip. Thus, both the displacements and the forces at the crack tip are calculated during a single

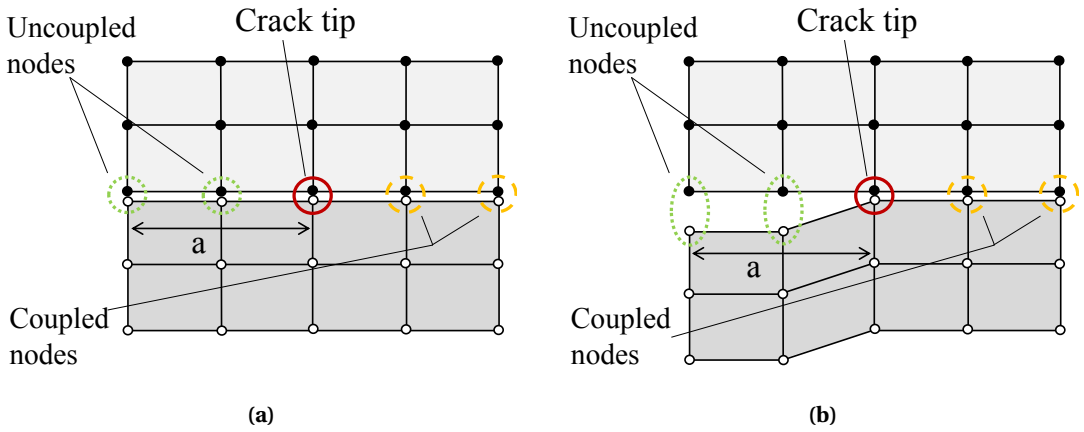


Figure 4.2: Finite element representation of an interfacial crack of length a. The undeformed configuration (a) corresponds to the case where the crack is closed. The deformed configuration (b) shows how the mesh opens under loading. The nodes circled by dotted lines are initially coincident but uncoupled. The nodes circled by dashed lines correspond to the interface between the two materials, where the upper and lower nodes are coupled by enforcing identical displacements.

finite element analysis. Using a polar coordinate system with the origin at the extended crack tip, the energy release rate is given by:

$$G = \lim_{\Delta a \to 0} \frac{1}{2\Delta a} \int_0^{\Delta a} \sigma_{yy}(\Delta a - r, 0)\, v_r(r,\pi)\, dr + \lim_{\Delta a \to 0} \frac{1}{2\Delta a} \int_0^{\Delta a} \sigma_{xy}(\Delta a - r, 0)\, u_r(r,\pi)\, dr \qquad (4.28)$$

where G is the total energy release rate, σ_{yy} and σ_{xy} are the normal and shear stress near the crack tip respectively, u_r and v_r are the relative sliding and opening displacements between points on the crack faces and Δa is the crack extension at the crack tip. This expression is valid for two-dimensional cracks. It is assumed that the crack surface is calculated as $\Delta a \times 1$ where the two-dimensional model has unit thickness. The energy release rate is expressed in J m^{-2}.

In the finite element analysis, the crack is modeled as a discrete discontinuity as shown in Fig. 4.2b. In the initial configuration, shown in Fig. 4.2a, the mesh is undeformed and the nodes at the crack faces coincide. The nodes ahead of the crack tip are tied together by coupling constraints. Under an applied load, the mesh is deformed and reaches a configuration where the crack opens (Fig. 4.2b). The fracture mode in a two-dimensional structure can be either a pure mode I crack with normal separation of the crack faces, a pure mode II crack with tangential motion of the crack faces or a mixture between mode I and mode II combining normal and tangential separation.

4.2.3 Calculation of strain energy release rate

To practically compute the energy release rate from a finite element discretization, Irwin's expression is written in terms of nodal forces and displacements near the crack tip. The procedure for calculating the energy release rate from a single finite element analysis for linear and quadratic elements is presented [77, 78]. In this procedure, the following assumptions are made:

1) the mesh size around the crack tip is uniform;

2) the normal and shear stress ahead of the crack tip are assumed to follow an inverse square root distribution in the immediate vicinity of the crack tip;

3) the displacements of the crack faces are determined by the element shape functions.

Linear quadrilateral element

Fig. 4.3a depicts the finite element discretization of an interfacial crack with the corresponding node names and coordinate system. The calculations are shown for the mode II contribution only. In mode I they are very similar. For the linear quadrilateral element L, the displacement interpolation function $u(x)$ on the i-j side is given by:

$$u(x) = \left[1 - \frac{x}{\Delta a}\right] u_i + \frac{x}{\Delta a} u_j \tag{4.29}$$

The relative tangential opening of the crack is given by:

$$u_r(r) = \frac{r}{\Delta a}(u_k - u_{k'}) \tag{4.30}$$

Ahead of the crack tip along the crack propagation direction, the near field shear stress σ_{xy} is assumed to follow an inverse square root distribution:

$$\sigma_{xy}(x, y = 0) = \frac{A_1}{\sqrt{x}} + A_2 \quad \text{for } x > 0 \tag{4.31}$$

where A_1, A_2 are unknown constants. The nodal forces F_{x_i}, F_{x_j} can be thought of as nodal forces acting at nodes i, j due to a prescribed stress distribution of the form in Eq. 4.31. Conversely, using these nodal forces, one can calculate the constants in the assumed stress distribution of Eq. 4.31 ahead of the crack tip along the crack line.

The stress distribution in Eq. 4.31 is valid only in the immediate vicinity of the crack tip since it is obtained from the near field solution at the crack tip. Also, since there are two unknown constants in the assumed distribution, two forces are sufficient to determine the constants. The two forces F_{x_i} and F_{x_j} computed from the elements K and L nearest to and around the crack tip can be used. In a 2D problem, the forces are given per unit thickness and have the dimension $\mathrm{N\,m^{-1}}$. The work done by the assumed stress distribution on the boundary displacements of elements K and L is equated to the work performed by the forces F_{x_i} and F_{x_j} on the displacements u_i and u_j as:

$$\int_0^{\Delta a} \sigma_{xy}(x)\, u(x) dx = -\left(F_{x_i} u_i + F_{x_j} u_j\right) \tag{4.32}$$

where Δa is the element length. Since a shear stress σ_{xy} causes reaction forces in the opposite x-direction, a negative sign appears in Eq. 4.32.

In order to express the stress field as a function of the reaction forces, it is necessary to express A_1 and A_2 versus the reaction forces. By substituting Eq. 4.29 in Eq. 4.32 and equating the multipliers of u_i and u_j:

$$A_1 = -\frac{3}{2\sqrt{\Delta a}}(F_{x_i} - F_{x_j}); \qquad A_2 = \frac{2}{\Delta a}(F_{x_i} - 2F_{x_j}) \tag{4.33}$$

The mode II component of the energy release rate is given by:

$$G_{II} = \lim_{\Delta a \to 0} -\frac{1}{2\Delta a} \int_0^{\Delta a} \sigma_{xy}(\Delta a - r) u_r(r) dr = \lim_{\Delta a \to 0} -\frac{1}{2\Delta a}\left[F_{x_i}\,(u_k - u_{k'})\right] \tag{4.34}$$

The same procedure is followed to calculate the energy release rate in pure mode I G_I, resulting in a total energy release rate for linear quadrilateral element given by:

$$G = \lim_{\Delta a \to 0} -\frac{1}{2\Delta a}\left[F_{y_i}\left(v_k - v_{k'}\right) + F_{x_i}\left(u_k - u_{k'}\right)\right] \tag{4.35}$$

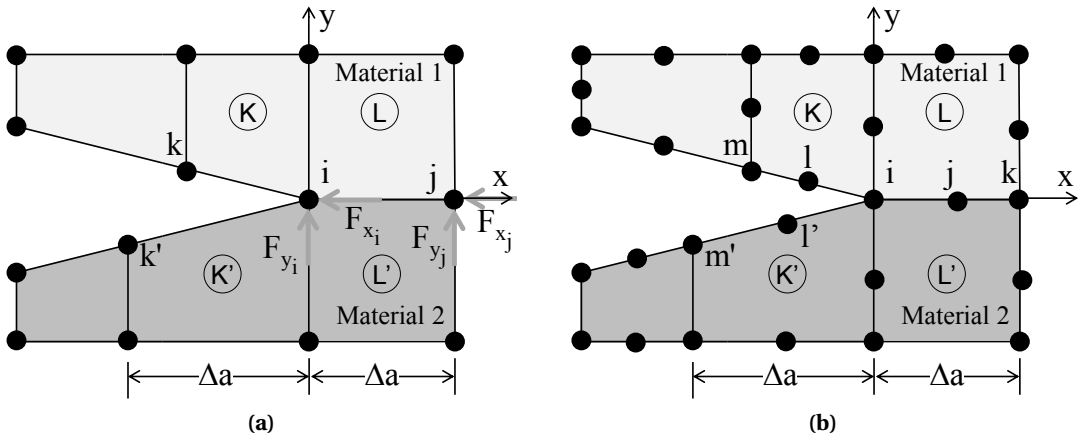


Figure 4.3: Linear (a) and quadratic (b) quadrilateral elements

Quadratic quadrilateral element

The notations for the quadratic quadrilateral element are shown in Fig. 4.3b. To describe the stress field in this element, a linear approximation of the near field stress distribution is made:

$$\sigma_y(x) = \frac{A_1}{\sqrt{x}} + A_2 + A3\sqrt{x} \tag{4.36}$$

The same procedure as for the linear quadrilateral element results in:

$$G = \lim_{\Delta a \to 0} -\frac{1}{2\Delta a}\left[F_{y_i}(v_m - v_{m'}) + F_{y_j}(v_l - v_{l'})\right] - \frac{1}{2\Delta a}\left[F_{x_i}(u_m - u_{m'}) + F_{x_j}(u_l - u_{l'})\right] \tag{4.37}$$

Under both small-scale contact and frictionless contact theory, this approach to calculate the energy release rate is valid.

4.3 Model and verification

Though analytical expressions for the crack driving force are available for some simple interface configurations, they involve complex mathematical derivation. For complicated geometries or

loading situations, analytical expressions are not available in the literature. The approach is thus to solve the problem numerically by means of a finite element analysis.

4.3.1 Finite element model

Fig. 4.4 describes the two-dimensional model of the package (not to scale), consisting of three components: the chip, the leadframe and the mold compound. The crack is shown as a white line in Fig. 4.4a. The two dashed boxes indicate partition of differently meshed domains. Indeed, due to the large scale difference, obtaining a mapped mesh in most of the regions requires transitions. The detail of the mesh transition around the crack tip is shown in Fig. 4.4b. Around the crack tip a very refined mesh is required in order to perform the energy release rate calculation. In addition, elements ahead and behind the crack tip have the same size, in order to directly apply the approach to calculate G shown in the previous section. Fig. 4.4c shows the deformation of the elements along the crack faces. The crack faces are in contact close to the crack tip (contact zone), where sliding dominates. Further away from the crack tip, close to the chip edge, both sliding and normal opening are shown.

Fig. 4.4a shows also the boundary conditions. A minimum number of boundary conditions is applied in order to avoid rigid body motion. This is based on the test methods that were used in the previous chapter, where the devices are either simply supported (standard temperature cycling) or prevented from deforming in one direction (fast temperature test). The loading consists of a uniform temperature applied to the structure. The structure is assumed stress-free at room temperature. The crack faces are prevented from interpenetrating by contact elements, governed by a contact penalty method. Frictionless contact is assumed.

The mold compound and the leadframe material are assumed isotropic. The viscoelasticity of the mold compound is neglected in this study. The chip is modeled as an orthotropic material, either silicon or silicon carbide. Silicon and silicon carbide are brittle materials. At room temperature, they fail with no observable plastic deformation.

The model dimensions are given in Tab. 4.5. Except for the outer dimensions, the model is fully parametric, allowing to vary geometrical parameters such as the chip width w_c and thickness t_c, or its distance w_s to the edge of the package. This ability will be used later on to propose design guidelines.

4.3.2 Displacement and stress fields along the crack and interface

To evaluate whether small scale contact theory or large scale contact theory are the most suitable in this situation, the displacement and stress fields are investigated for a relatively long

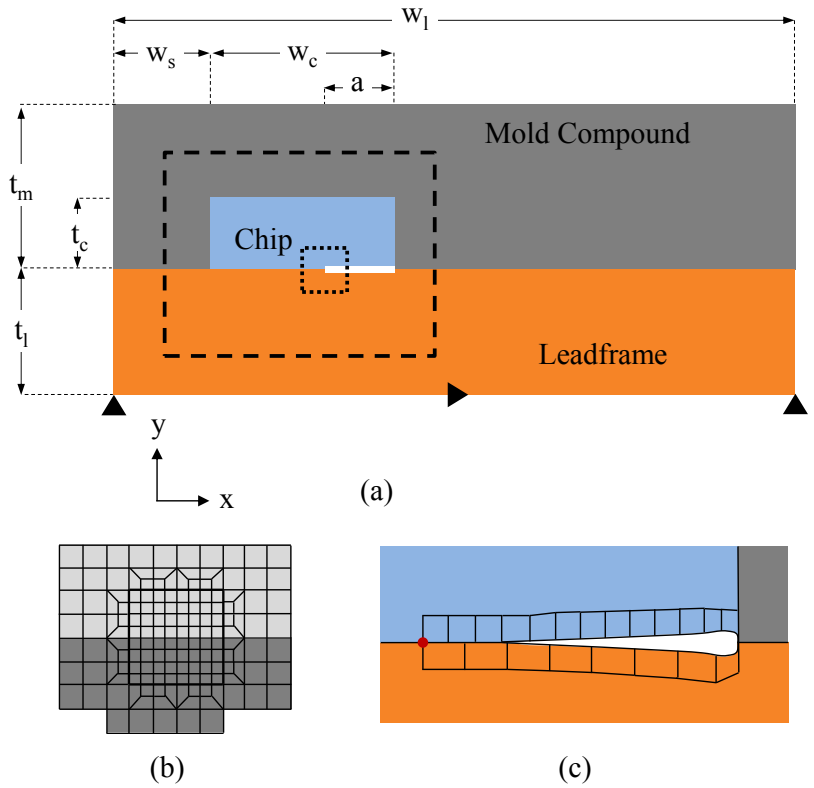


Figure 4.4: Geometrical model used for the finite element simulation (not to scale). (a) Mold compound (gray), chip (blue), leadframe (orange) and crack (white) are shown. The dashed boxes indicate the domains of different mesh size. (b) Detail of the mesh transition around the crack tip. (c) Detail of the element deformation around the crack tip (red dot).

Figure 4.5: Model dimensions in µm. The external boundaries of the model are fixed, while the inside dimensions are parametric.

	Constant		Parametric				
	t_m	w_l	t_c	t_l	w_s	w_c	a
Default	3130	7925	110	1170	1000	635	20 to 130
Minimum	3130	7925	50	300	1000	635	20
Maximum	3130	7925	350	2000	7000	6000	20% w_c

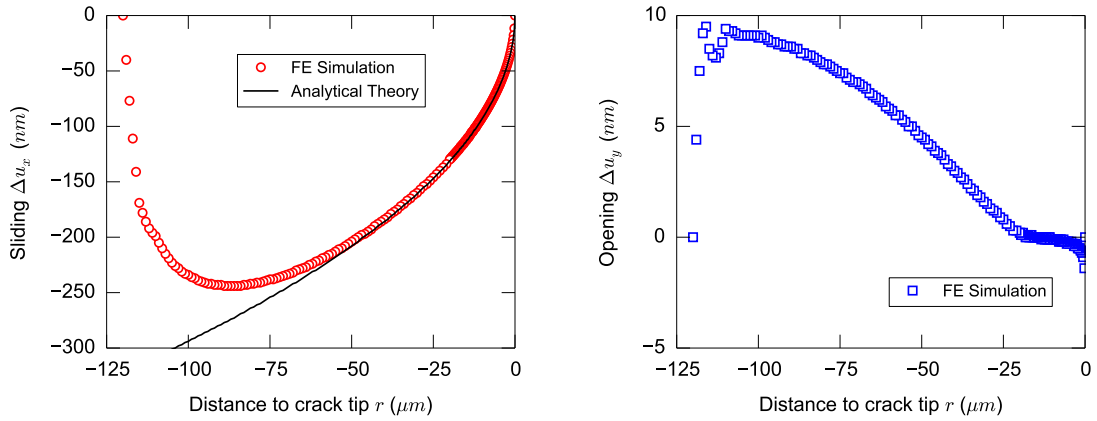


Figure 4.6: Sliding and opening of the crack faces. (a) Sliding of the crack faces $\Delta u_x = u_x^{top} - u_x^{bot}$. The analytically calculated sliding agrees well with the simulated behavior in the neighborhood of the crack. The subsequently observed discrepancy is due to the specific boundary condition at the chip edge. It is required that leadframe, mold compound and chip material stay coincident. (b) Opening of the crack faces $\Delta u_y = u_y^{top} - u_y^{bot}$. In the neighborhood of the crack, up to 20 µm contact is observed. Afterward a small opening, one order of magnitude smaller than the sliding, is observed.

crack of 120 µm at the interface between leadframe and chip. The default geometry is used. To easily compare the results with theory, both materials are assumed isotropic. The worst case properties leading to the largest Dundurs parameter are used for silicon carbide based on the calculation of its uniaxial properties ($\beta = 0.155$, $\varepsilon = 4.96 \times 10^{-2}$).

Fig. 4.6b shows the relative displacements of the crack free faces. An interpenetration of 0.5 nm occurs in a confined region of 3 µm close to the tip. This interpenetration is allowed by the contact penalty method. In a region up to about 20 µm away from the crack tip, the crack faces are in close contact with negligible interpenetration. Thus the contact zone size for this crack length is about 20 µm. For distances larger than 20 µm, the crack faces slowly open to reach a maximal normal opening of 10 nm. The normal opening reaches its maximum in the neighborhood of the chip edge where boundary conditions require that the chip edge, leadframe and mold compound stay coincident, not allowing any opening. This condition is not necessarily representing the reality, as it has been observed on some failure images that a short crack may form at the mold compound/leadframe interface.

Fig. 4.6a shows the relative sliding of the crack faces versus the distance to the crack tip. The sliding is increasing proportionally to the crack tip distance to reach its maximum at about 90 µm from the crack tip with a value of 250 nm. The sliding is again zero at the chip edge due to the boundary conditions. The leadframe material moves relative to the chip in the positive x-direction, which is expected due to their respective coefficient of thermal expansion.

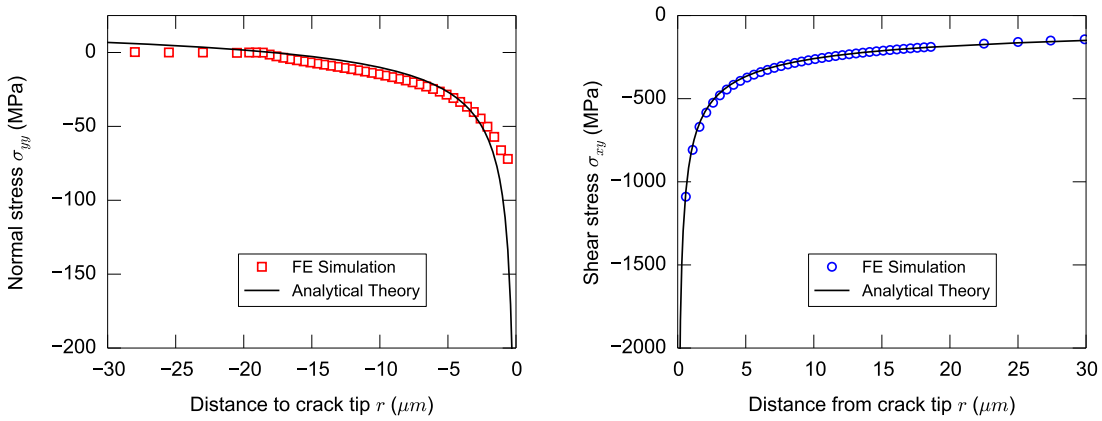


Figure 4.7: Analytical and simulated normal stress ahead and behind the crack tip. The coordinate system has its origin at the crack tip. (a) The analytical normal stress solution (full line) behind the crack tip is in good agreement with the simulated stress in the contact zone. (b) The analytical shear stress inverse square root dependence ahead of the crack tip agrees well with the simulation results.

From Fig. 4.6, it is observed that the maximal normal opening is one order of magnitude lower than the maximal sliding. In the crack tip region, sliding dominates over normal opening. As a result, the mode II fracture dominates the fracture process in this structure. The size of the contact zone, evaluated at 20 µm for a 120 µm crack, cannot be neglected. Therefore, small scale theory cannot be applied. However, as a frictionless contact has been implemented, the stress field is expected to follow a square-root singularity as demonstrated in the section concerning the friction contact. The predicted sliding according to the contact theory agrees well with the simulated one. The corresponding constants are shown in Tab. 4.1.

Fig. 4.7a shows the normal stress along the crack faces and the predicted values according to the contact theory. The normal stress field is well predicted in the contact zone. Due to the frictionless contact a zero shear stress is expected along the crack faces. In the simulation a zero shear stress is actually reached few elements away from the crack tip. Fig. 4.7b describes the shear stress along the interface between the leadframe and the chip. The shear stress follows the inverse square root singularity predicted by the large scale contact theory in the contact zone. The normal stress along the interface reaches a small constant value of 10 MPa far away from the crack tip. This non-zero value is due to the uniform temperature loading of the structure.

The stress and displacement fields follow the square root dependence on the crack tip distance. Due to the presence of a large contact zone at the crack tip, small-scale theory is not applicable anymore. As the crack faces are in contact, mode II dominates.

Table 4.1: Constants describing the stress and displacement fields according to the contact theory, in the special case of a frictionless contact. The only fitting parameter is K_{II}.

Constant	Value
K_{II}	$-65\,\mathrm{MPa}\sqrt{\mathrm{mm}}$
λ	0.5
β	-0.15
γ	$3.59\times10^{-5}\,\mathrm{MPa}^{-1}$

4.4 Factors influencing degradation

Various parameters can trigger degradation. The following parameters have been identified to be significant for crack growth:

- Loading conditions
- Material properties of the chip and mold compound
- Geometry parameters

The crack driving force is evaluated at the maximum loading temperature. As already mentioned, mode II loading dominates. As a result, it is sufficient to examine only the crack driving force change with the parameter and to neglect the mode mixity change.

4.4.1 Influence of loading conditions

The structure is mainly subjected to temperature loading. The mismatch of the thermal expansion coefficients between the materials induces thermal strains in the structure under thermal loading. The effect of temperature on crack driving force is investigated here. Note that the material properties are temperature independent. The simulated structure has the default dimensions given in Tab. 4.5. The result shows the effect of temperature loading changes for silicon carbide, with all other parameters given.

Fig. 4.8a shows the crack driving force versus crack length parameterized by the applied temperature difference ΔT. At a given temperature difference, the crack driving force increases slightly to reach a peak. Then it decreases steadily. The initial increase is predicted by [55]. It was shown that for a film on a substrate, the energy release rate first increases and then reaches a steady value, depending only on the film mechanical properties, its thickness and the remote applied stress. The steady value is reached when the crack tip is located far enough from the edge. In the study presented here, the crack driving force decreases after reaching a maximum

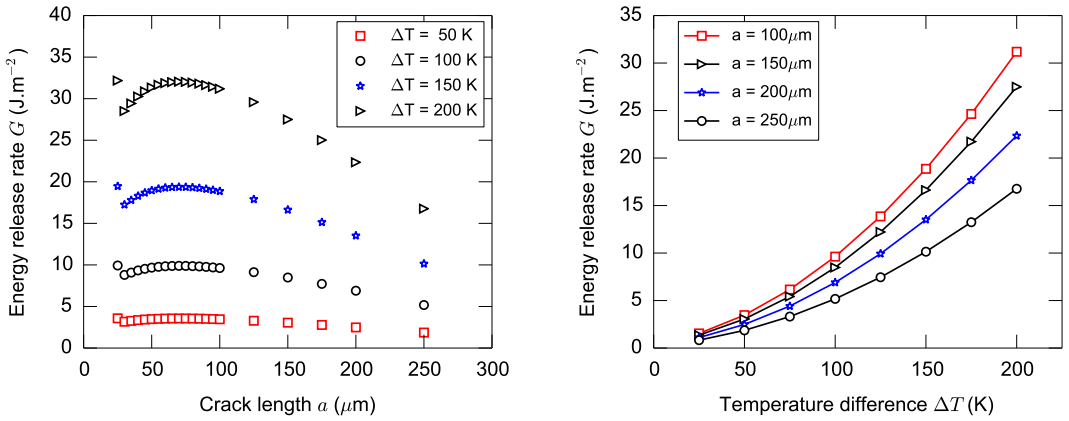


Figure 4.8: Temperature effect on the crack driving force. The default dimensions are used. The results are shown for silicon carbide chip. The maximum crack size (250 µm) corresponds to approximately 40 % of the chip width. (a) The crack driving force increases slightly to reach a maximum. It then decreases linearly. The initial increase might be caused by the proximity of the chip edge and the specific boundary conditions. (b) The crack driving force increases significantly. It has a ΔT^2 dependence.

because the geometry is finite.

Fig. 4.8b shows the crack driving force versus the applied temperature difference parameterized by the crack length. The crack driving force increases non linearly. This dependence can be retrieved by considering an analytically solved problem. Erdogan [79] derived the stress field solution for two bonded semi-infinite plates with a center crack under uniform thermal loading. The stress depends linearly on the temperature difference ΔT between the operating temperature and the bonding temperature. It results in the real and imaginary parts of the complex stress intensity factor being proportional to ΔT. As mentioned in Section 4.1 the energy release rate is proportional to the square of the stress intensity factor. Thus it is also proportional to the square of the applied temperature difference.

4.4.2 Influence of mechanical material properties

Influence of the mold compound

The structure consists of three materials. Their respective elastic properties impact on the global stiffness of the structure, resulting in different deformations. The effect of the Young's modulus of the mold compound is investigated here. The simulated structure has default dimensions (Tab. 4.5). It is subjected to a uniform temperature difference of 200 K. The results

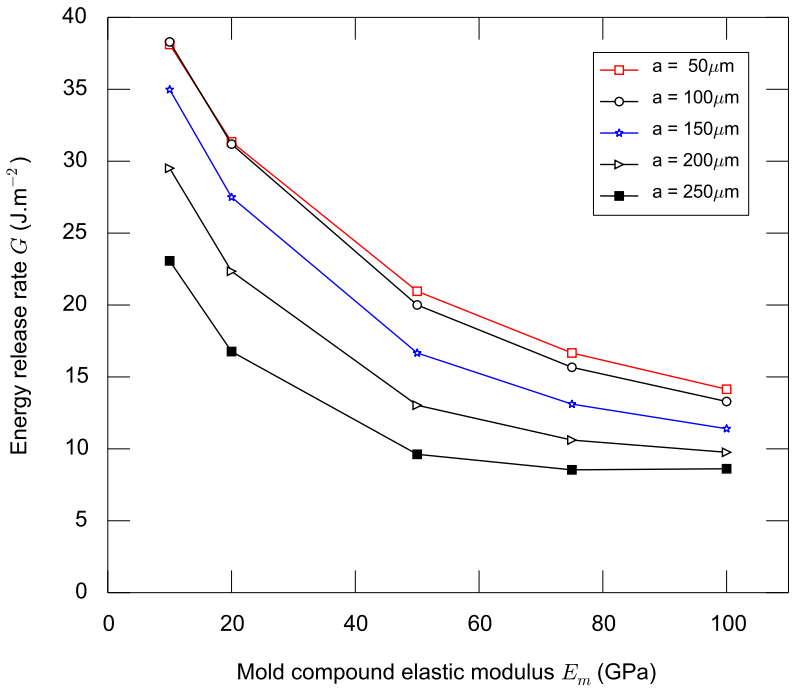


Figure 4.9: Effect of mold compound properties. For values of elastic modulus below 50 GPa, the crack driving force is significantly impacted.

shown here are for a chip made of silicon carbide.

Fig. 4.9 shows the energy release rate versus the elastic modulus of the mold compound, parameterized by the crack length a. The crack driving force decreases significantly for an elastic modulus in the range of 10 GPa to 50 GPa. For an elastic modulus in the range of 50 GPa to 100 GPa, the crack driving force decreases slightly. It stays constant for the longest considered crack. A stiffer mold compound results in a lower crack driving force. The properties of the mold compound can be modified by adding more or less filler to the polymer melt before curing. Usually adding filler to the polymer causes a stiffer behavior [80].

Influence of the chip material

Similarly to the mold compound the elastic properties of the chip influence the structural behavior. Here for comparison purpose, the chip material is assumed isotropic and its elastic modulus is varied. The mold compound and leadframe properties are given realistic values. The structure is subjected to a uniform temperature difference ΔT =200 K.

Fig. 4.10a depicts the crack driving force versus the chip elastic modulus, parameterized by the crack length. The crack driving force increases significantly. The modulus of silicon ranges

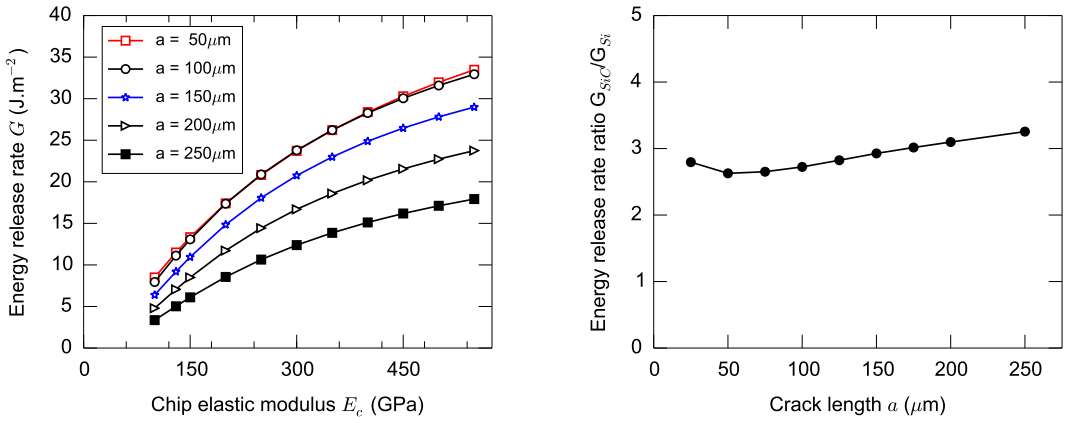


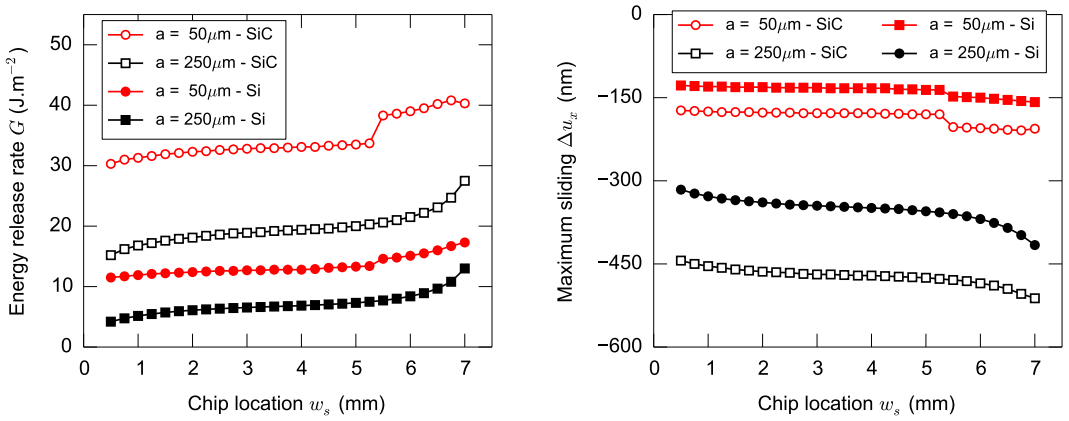
Figure 4.10: Effect of chip properties. (a) The crack driving force increases significantly. Lower elastic moduli are beneficial to reliability. (b) Ratio of the energy release rate of SiC over the one of Silicon (Si). The ratio is roughly constant and equal to three.

from 130 GPa to 180 GPa [31] while the one of silicon carbide ranges from 472 GPa to 544 GPa. Thus using silicon carbide results in a larger energy release rate. Fig. 4.10b depicts the ratio of energy release rate in a structure simulated with orthotropic silicon to orthotropic silicon carbide. It indicates that the energy release rate for silicon carbide is roughly three times larger than the energy release rate for silicon.

4.4.3 Influence of the geometry

Influence of the chip location w_s

The default geometry of the structure is used, except for the parameter reflecting the distance to the side w_s (Fig. 4.4). It is varied from 0.5 mm to 7 mm. Fig. 4.11a shows the evolution of the crack driving force versus the chip location for various crack lengths and chip materials. The crack driving force increases with the distance to the left side. It stays constant when the chip is located in the middle of the leadframe (w_s ranging from 2.5 mm to 5 mm. For Si, the crack driving force is multiplied by 3 when w_s changes in its range. For SiC, the crack driving force is multiplied by 1.8. As already mentioned, the lower crack face (leadframe) displaces toward the right compared to the upper crack face (chip) for a right crack. It means that as the distance to the left side increases, the distance of the crack to the right side decreases. Thus when the lower face displaces toward the right side, it must displace less material when the chip is located on the right side than when it is located on the left side of the leadframe. As the chip is on the left of the leadframe, the material resistance encountered by the lower face to slide is much larger than if it were located on the right side. As the energy release rate is proportional to the



(a) **(b)**

Figure 4.11: (a) Effect of chip location on the leadframe for silicon and silicon carbide parameterized by the crack length a. For a crack growing on the right side of the chip, the energy release rate increases if the chip is moved from left to right, remains steady when the chip is in the center of the leadframe and increases further. (b) Evolution of the maximum sliding of the crack faces versus the chip location. The energy release rate and the maximum sliding of the crack faces are linearly correlated.

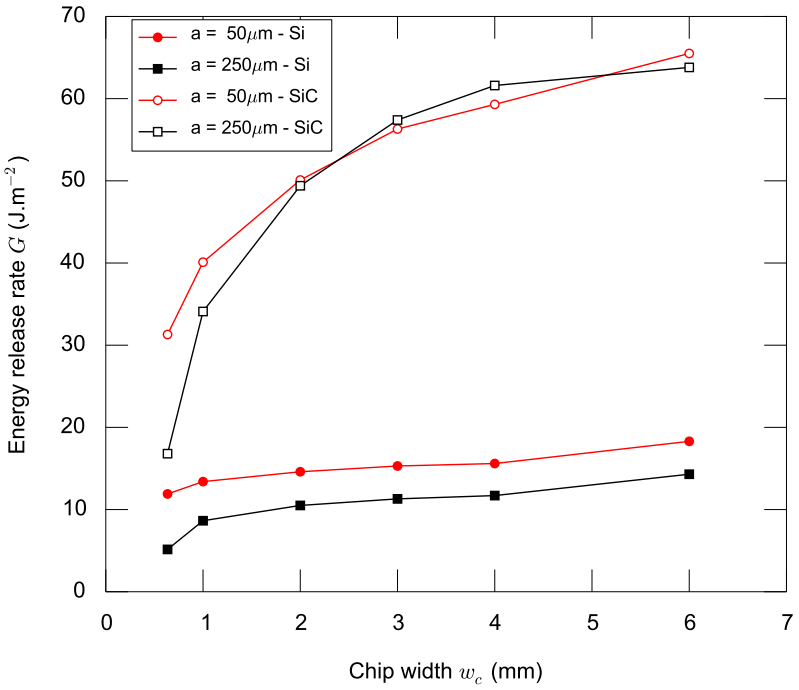


Figure 4.12: Effect of chip width for silicon. The energy release rate increases as the chip width w_c increases.

sliding magnitude, a crack on the right entails a larger energy release rate than a crack on the left of the leadframe. Fig. 4.11b depicts the evolution of the maximum sliding along the crack face versus the chip location. This correlation means that changing the location of the chip primarily influences the sliding. The force at the crack tip is not influenced by changing the chip location.

The dependence of the crack driving force on w_s can be modeled by a continuous function for a crack length of $a = 250$ µm for Si:

$$f_{w_s} = \begin{cases} 1.2765 \ln w_s + 5.1437 & 0.5 \le w_s \le 4.0 \\ 0.3502 w_s + 5.5125 & 4.0 \le w_s \le 4.5 \\ 0.6542 w_s^2 - 5.9347 w_s + 20.5470 & 4.5 \le w_s \le 7.0 \end{cases} \quad R^2 = 0.99 \text{ over the full range.} \tag{4.38}$$

The coefficient of determination is calculated as:

$$R^2 = 1 - \sum (y_i - f_i)^2 / \sum (y_i - \bar{y})^2 \tag{4.39}$$

where y_i are the simulated values of the energy release rate, f_i the values predicted by the regression model and $\bar{y}$ the mean of the simulated values.

The dependence of the crack driving force on w_s can be modeled as a natural logarithm function for a crack length of $a = 250$ µm for SiC:

$$f_{w_s} = 1.9956 \ln w_s + 16.6880; \quad 0.5 \le w_s \le 7; \quad R^2 = 0.997. \tag{4.40}$$

Influence of the chip width w_c

The default geometry of the structure is used, except for the chip width w_c parameter. The chip width is varied from 0.635 mm to 6 mm. Fig. 4.12 shows the variation of crack driving force versus the chip width, parameterized by the crack length a. The crack driving force increases steeply for small chip width and slowly for larger chip width. The crack driving force is multiplied by 2.8 for Si and by 3.8 for SiC. The curvature of the substrate modifies the stress state around the interface and is thus related to the crack driving force. The presence of a chip with small width influences only locally the curvature of the substrate, while a wider chip modifies the value of the global curvature of the substrate. This explains the rate of change of G with chip width for small crack, which is observed to increase steeply for small chip width and to increase slowly for large chips.

The dependence of the crack driving force on w_c can be modeled by a continuous function for

a crack length of $a = 250$ µm for Si:

$$f_{w_c} = \begin{cases} 3.5736 \ln w_c + 7.9507 & 0.635 \leq w_c \leq 3 \\ -0.139 w_c + 12.294 & 3 \leq w_c \leq 4 \\ 0.4659 w_c^2 - 3.3956 w_c + 17.866 & 4 \leq w_c \leq 6 \end{cases} \quad R^2 = 0.94 \text{ over the full range.} \tag{4.41}$$

The dependence of the crack driving force on w_c can be modeled as a natural logarithm function for a crack length of $a = 250$ µm for SiC:

$$f_{w_c} = 20.9290 \ln w_c + 31.3360; \quad 0.635 \leq w_c \leq 6; \quad R^2 = 0.95. \tag{4.42}$$

Influence of the chip thickness

The default structure is used, except for the chip thickness parameter. It is varied from 50 µm to 350 µm. Fig. 4.13 depicts the crack driving force evolution versus the chip thickness. It increases non linearly versus chip thickness. The crack driving force is multiplied by 5.7 for Si and 3.8 for SiC. The increase in chip thickness results in an increase of the structure stiffness.

The dependence of the crack driving force on t_c can be modeled as a natural logarithm function for a crack length of $a = 250$ µm for Si:

$$f_{t_c} = 13.467 + 3.8713 \ln t_c; \quad 50 \times 10^{-3} \leq t_c \leq 350 \times 10^{-3}; \quad R^2 = 0.99. \tag{4.43}$$

Likewise, the dependence of the crack driving force on t_c can be modeled as a natural logarithm function for a crack length of $a = 250$ µm for SiC:

$$f_{t_c} = 4.4783 \ln t_c + 25.42; \quad 50 \times 10^{-3} \leq t_c \leq 350 \times 10^{-3}; \quad R^2 = 0.95. \tag{4.44}$$

Influence of leadframe thickness

The default structure is used, except for the leadframe thickness. It is varied from 0.5 mm to 2 mm. Fig. 4.14 shows the change in crack driving force versus the leadframe thickness. The crack driving force increases slightly with the leadframe thickness. The increases is more pronounced for silicon carbide than for silicon. The crack driving force is multiplied by 1.2 for Si and 1.3 for SiC.

The dependence of the crack driving force on t_l can be modeled as a second order polynomial

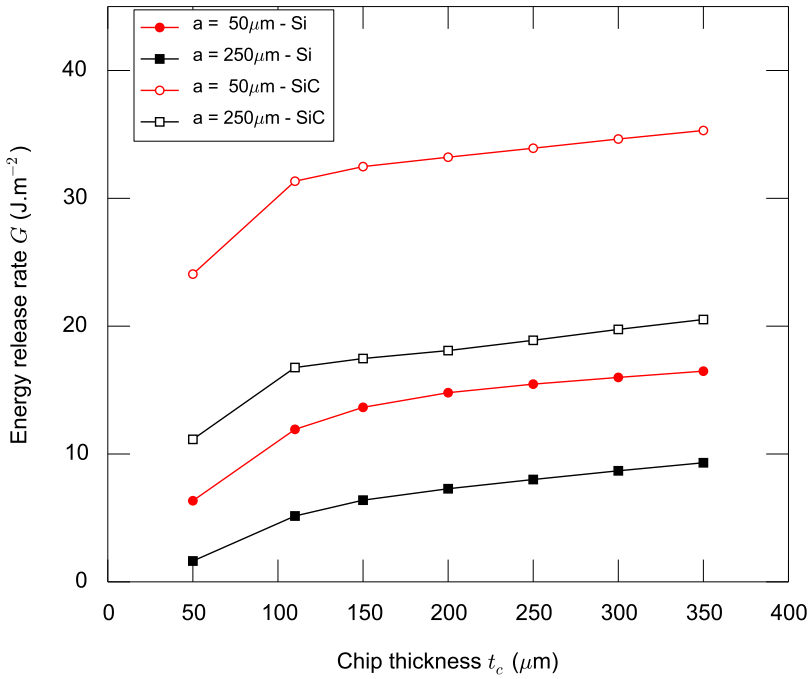


Figure 4.13: Effect of chip thickness. The energy release rate increases as the chip thickness increases.

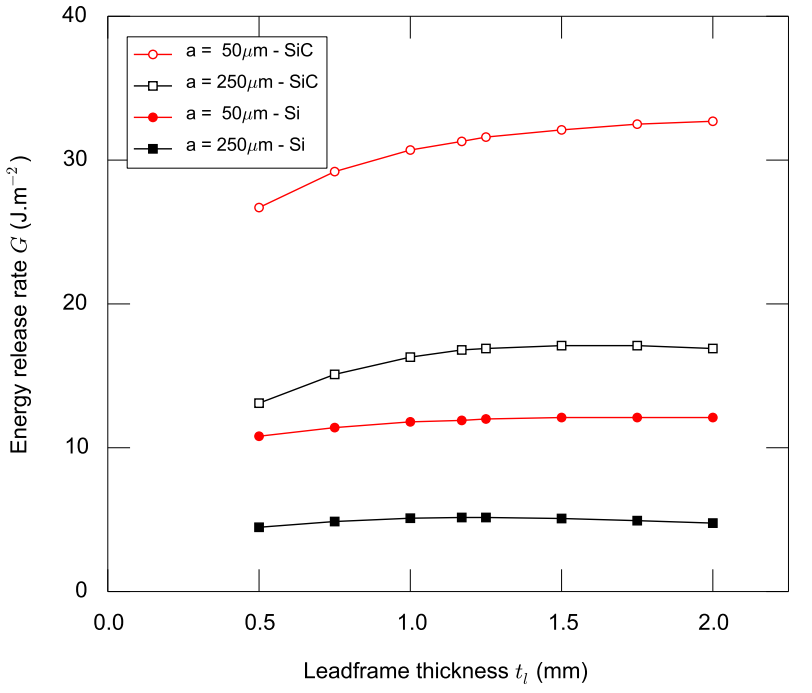


Figure 4.14: Effect of leadframe thickness. The energy release rate increases as the leadframe thickness increases for SiC. For Si, it reaches a maximum at roughly 1.2 mm.

function for a crack length of $a = 250$ µm for Si:

$$f_{t_l} = -1.099\,t_l^2 + 2.9289\,t_l + 3.2289; \quad 0.3 \leq t_l \leq 2; \quad R^2 = 0.98. \tag{4.45}$$

The dependence of the crack driving force on t_l can be modeled as a second order polynomial function for a crack length of $a = 250$ µm for SiC:

$$f_{t_l} = -4.3346\,t_l^2 + 13.4370\,t_l + 7.0656; \quad 0.3 \leq t_l \leq 2; \quad R^2 = 0.97. \tag{4.46}$$

4.4.4 Guidelines

Guidelines for minimization of the energy release rate for various configurations can be inferred from the previous study. In this section, we consider a crack length of 250 µm, which is the critical crack length in the application when considering an intermediate chip width of 2.5 mm. Assuming that the energy release rate is a linear combination of the previously determined f_{t_l}, f_{t_c}, f_{w_c} and f_{w_s} and normalizing the dependency, the following model is proposed:

$$G = \alpha \frac{f_{t_l} - \bar{f}_{t_l}}{\sigma_{f_{t_l}}} + \beta \frac{f_{t_c} - \bar{f}_{t_c}}{\sigma_{f_{t_c}}} + \gamma \frac{f_{w_s} - \bar{f}_{w_s}}{\sigma_{f_{w_s}}} + \lambda \frac{f_{w_c} - \bar{f}_{w_c}}{\sigma_{f_{w_c}}} + \eta \tag{4.47}$$

where the bar denotes the average of the quantity and σ its standard deviation. The parameters α, β, γ, λ give the relative significance of each geometrical parameter and are reported in Tab. 4.2. This is only a first approximation as the energy release rate does not linearly depend on each parameter. Keeping this in mind, the following ranking can be done. For Si, the parameters are ranked as:

1) chip thickness;
2) chip width;
3) distance to the side;
4) leadframe thickness.

The parameters having the largest influence are the chip thickness and chip width, which are roughly three times more significant than the influence of the leadframe thickness and the distance to the side dependencies. For SiC, the significance of the parameter influence is ranked as:

1) chip width;
2) leadframe thickness;
3) chip thickness;

Table 4.2: Significance of the geometrical parameters for Si and SiC.

	Si	SiC
$\alpha \equiv t_l$	0.77	2.30
$\beta \equiv t_c$	2.78	1.81
$\gamma \equiv w_s$	0.83	0.79
$\lambda \equiv w_c$	2.51	14.56
η	7.68	21.91

4) distance to the side.

The most significant dependency is the one on chip width, which is roughly six times higher than the other dependencies.

Linear elastic fracture mechanics is a valuable tool to predict the worst case situation in a structure as a first approximation. Parametric studies can be performed with reasonable effort. The effect of various parameters on interface crack propagation can be predicted. The change of crack driving force over one temperature cycle can be interpreted in terms of lifetime by considering the Paris law [81]. The crack growth rate is a power law of the energy release rate. This study is limited in its interpretation due to the absence of interfacial toughness data. However, it is known that for interfacial cracks, the toughness is dependent on the mode mixity and the temperature. Here the mode mixity is not an issue and except for the loading conditions, all temperature differences are kept identical, which justifies the comparability of the data. The obtained results are to be considered with care. Indeed, influence of residual stress and mold compound viscoelasticity have not been taken into account. Neglecting mold compound viscoelasticity leads to overestimation of the energy release rate [82].

5

Modeling interfacial delamination under thermal fatigue

In the previous chapter, the influence of key geometrical parameters on the energy release rate was studied. However, this approach does not allow direct prediction of the crack propagation for a given number of cycles. To do so, additional hypotheses are required. Commonly, the Paris law is used. In this chapter, an alternative approach based on the Cohesive Zone (CZ) technique is proposed, which is able to predict crack initiation as well as propagation.

A material subjected to cyclic loading will fail at a load much lower than that required to cause failure during monotonic loading. Such failures are called fatigue failures [83]. A typical loading profile for such a fatigue failure is shown in Fig. 5.1a. Fatigue crack growth rates in metals have been shown experimentally [25] to follow a three-stage behavior depending on the stress intensity factor range ΔK, as shown in Fig. 5.1b. ΔK is linked to the crack length a and the applied stress σ_a. In the first region, below a threshold ΔK_{th}, the crack will not grow, except for the special case of short cracks. At intermediate values of ΔK, the crack growth rate increases linearly in a log-log representation with the applied ΔK. It deviates from the linear behavior at low and high ΔK. At high ΔK, the crack growth rate accelerates significantly. The intermediate region is usually modeled using the phenomenological Paris law [25, 84], which relates the applied stress intensity factor range ΔK to the fracture crack growth rate per cycle $\frac{da}{dN}$ using a power law. The Paris law is valid only under the strong assumption of LEFM, that is small-scale

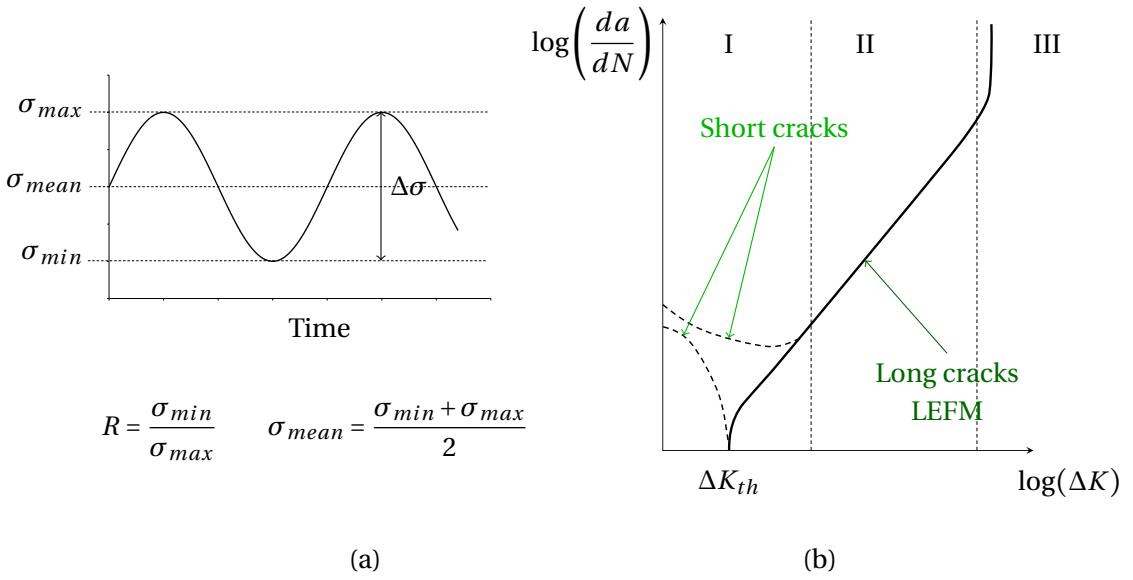


Figure 5.1: (a) Typical loading profile leading to fatigue failure. σ_u is the tensile strength of the material, σ_{min} and σ_{max} the minimum and maximum applied stress, R the stress ratio. (b) Schematic of the typical fatigue crack growth behavior in log-log scale. Dashed lines represent the possible behavior of short cracks, while the full line depicts the expected behavior for long cracks under constant amplitude loading. Stage II for long cracks is modeled by the Paris law.

yielding and similitude conditions [85]. Additionally, caution is advisable as it was suggested that cracks can be classified [86] as:

- microscopically short cracks where continuum mechanics is no longer applicable because the crack is about the length of the grain size,
- mechanically short cracks where small-scale yielding does not hold anymore and more advanced theory such as elastic plastic fracture mechanics have to be considered,
- physically short cracks (*e.g.* ≤0.5 mm) where the similitude assumption does not hold anymore.

All three types of short cracks have been observed to grow faster than long cracks subjected to the same driving force. Additionally, they might exhibit subcritical crack growth, *i.e.* growth under the ΔK_{th} identified for long cracks. Various expressions based on the Paris law have been proposed to model specific effects such as the stress ratio effect [87,88], large scale yielding [89], crack retardation [90], crack closure [91,92], and short cracks [93].

To model interfacial crack propagation under cyclic loading, the classical stress intensity factor cannot be used due to the presence of a bimaterial interface. The energy release rate range ΔG is used instead [94]. In the studied configuration, given the interfacial delamination area with respect to the surrounding thin backside metalization layers, the question arises whether the

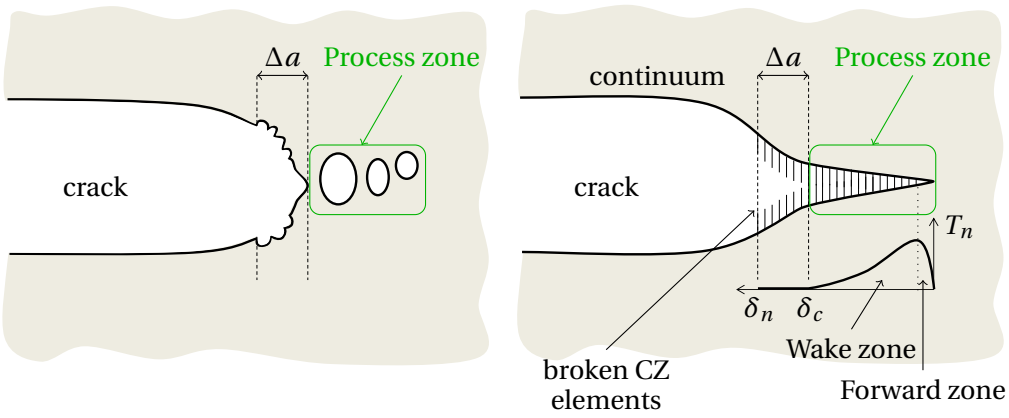
problem should be treated as a mechanically short crack. Additionally, the surrounding layers behave plastically. In order to be able to predict both initiation and propagation without being limited by the type of the surrounding materials, propagation is modeled using the Cohesive Zone (CZ) approach.

5.1 Introduction to cohesive zone models

In most materials, a crack is surrounded by a fracture process zone, where plastic yielding, micro-cracking, void growth and coalescence take place [95] as shown in Fig. 5.2. Depending on the size of this region compared to the crack length, it might not be possible to neglect it, thus rendering the use of LEFM inappropriate. Barenblatt [96], Dugdale [97] and Hillerborg [98] introduced the first concepts of the CZ models. In the CZ approach, the various processes occurring at the crack tip are modeled by the use of a Traction-Separation Law (TSL). The fracture process zone, located ahead of the real crack tip, is a region where the material degradation is modeled by an actual opening. As the crack opens under the action of loads, the opening is resisted by the material due, for instance, to cohesion at the atomic scale and interlocking of grains [85, 99]. The CZ approach describes the actual physical processes occurring in the fracture process zone at a larger scale: it does not take into account atomic separation, voids or micro-cracks, but gathers all these processes into a single TSL [95]. As the CZ approach represents all processes occurring in the fracture process zone, it is also independent of the sample geometry, the crack classification and the crack tip plastification. It is a unified treatment of crack initiation and propagation [99]. CZ models allow the prediction of crack growth from the knowledge of the properties of the individual materials and the interface fracture energy. Such a model is thus geometry independent and easily transferable from geometry to geometry.

CZ models are typically thought to be used in combination with finite element analysis. The cohesive behavior can be introduced either as interface element [101] or as contact interaction [102]. The CZ elements have to be present all along the crack path. Several solutions can be adopted. If the crack path is known as in the case of a very weak interface, only the crack path is meshed with CZ elements. In case of an unknown path, one can use material strength concepts to determine the probable crack propagation direction and locally remesh the model [103]. Another computationally expensive possibility is to introduce CZ elements along the borders of all continuum elements [104]. If a CZ has been initially developed to model fracture in homogeneous material, the concept is naturally applied to interfacial crack modeling.

CZ models can be classified in two categories [105]: displacement-based and potential-based models. The displacement-based models are an intuitive approach of the problem and thus are used here to explain the principle of the CZ approach.



(a) Reality (b) Idealization

Figure 5.2: The fracture process zone is shown by a rounded box. (a) Ductile fracture mechanism. Voids are nucleated at the crack tip due to the high stress triaxiality. Growth and coalescence of the voids result in crack growth. (b) Idealization by the use of cohesive zone representation. The fracture process zone consists of two zones: the wake zone, where intrinsic energy dissipation opposes the propagation (closure, blunting, oxidation) and the forward zone where extrinsic energy dissipation activates phenomena such as void coalescence or micro-cracking (adapted from [100]).

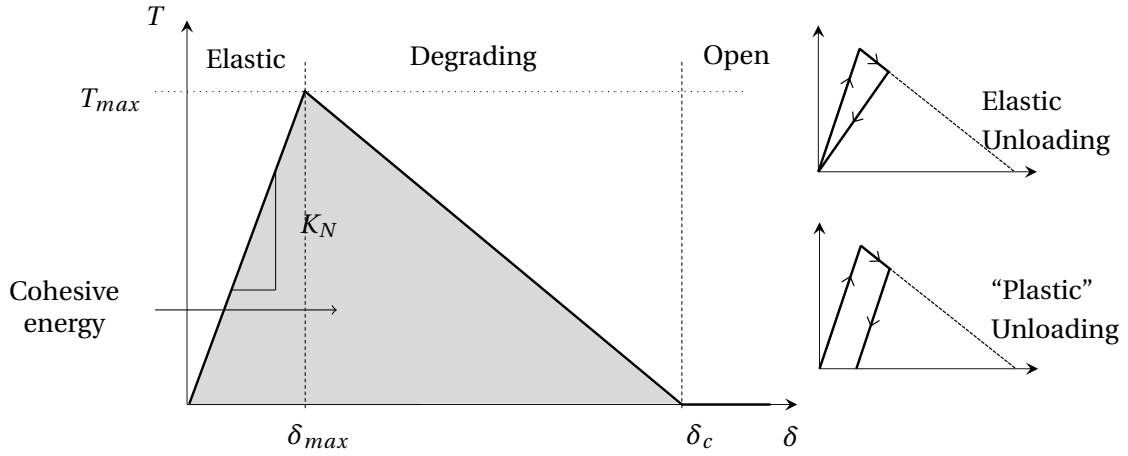


Figure 5.3: Bilinear traction-separation law.

5.1.1 Monotonic cohesive zone models

Displacement-based models

Fig. 5.3 shows a typical bilinear TSL. An opening value equal to the critical separation δ_c corresponds to a fully degraded contact *i.e.* no load bearing capacity. The slope denoted as K_N is often introduced in order to avoid numerical issues between the CZ elements and the surrounding continuum elements [100]. Once the maximum bearable traction T_{max} is reached, the element behavior softens, representing the progression of the specific damage mechanism, such as void coalescence for ductile fracture [100]. Generally the work required to create a new surface corresponds to the fracture energy and is obtained from the area under the curve. It corresponds to the critical energy release rate G_c of the material:

$$G_c = \int_0^{\delta_c} T(\delta) d\delta. \tag{5.1}$$

Various shapes of the TSL have been used in literature. Some authors mention that the shape must be chosen depending on whether ductile or brittle fracture occurs, arguing that in ductile fracture the main parameters are the fracture energy and the tensile strength [106–108] whereas in brittle fracture the actual shape of the TSL plays a much bigger role [108, 109]. Ductile fracture means large displacements and presence of dislocation while brittle fracture is characterized by the presence of micro-cracks [108]. The role of the TSL shape has been investigated by [107, 110–112]. Chandra *et al.* [112] have shown that in the case of composites, the TSL shape is significant to accurately simulate the interface. In addition, the shape of the TSL is reported to significantly influence accuracy and convergence by [101, 113]. Fig. 5.4 shows various shapes of TSL. An exponential TSL [114] is optimal for accuracy but computationally expensive while bilinear shapes [115, 116] offer the best trade-off between accuracy and rate of convergence [101]. Trapezoidal shapes [107, 117] are the least advisable in terms of both accuracy and convergence stability [101].

Displacement-based models are performing well in the case of pure mode I or pure mode II loading. However they are usually not thermodynamically consistent in case of arbitrary mixed-mode conditions [101, 105], especially when mode II fracture energy is different from mode I fracture energy, which is often the case. Indeed, a change of the loading mode during separation may result in apparent recovery. Fig. 5.5 depicts this situation. The element is first loaded in mode A and is fully degraded when the displacement reaches $\delta_{c,A}$. The loading mode is suddenly changed to mode B, which has a different TSL. The current effective displacement $\delta_{c,A}$ corresponds to a not yet open contact, which leads to false conclusion. Dependence on mode-mixity is typically linked to changes of damage mechanisms acting at the interface [118].

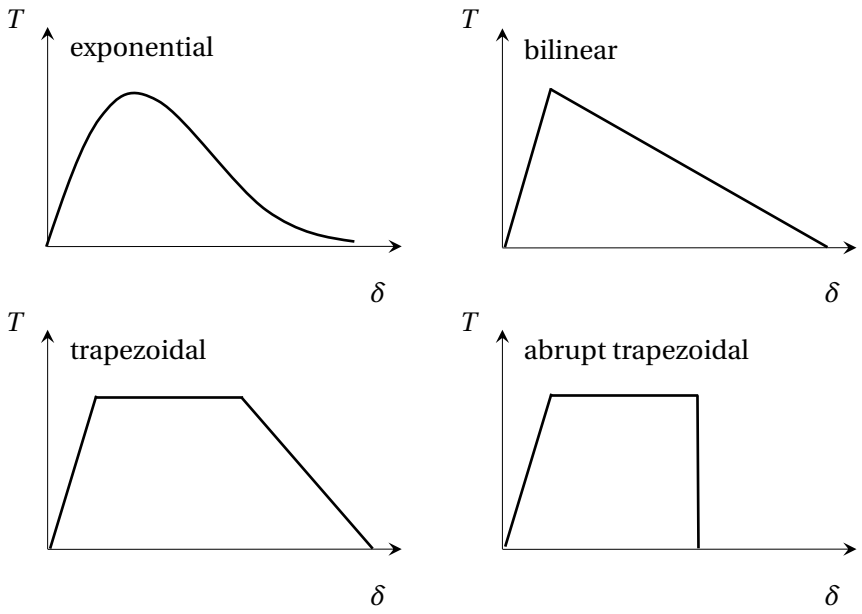


Figure 5.4: Various traction separation laws.

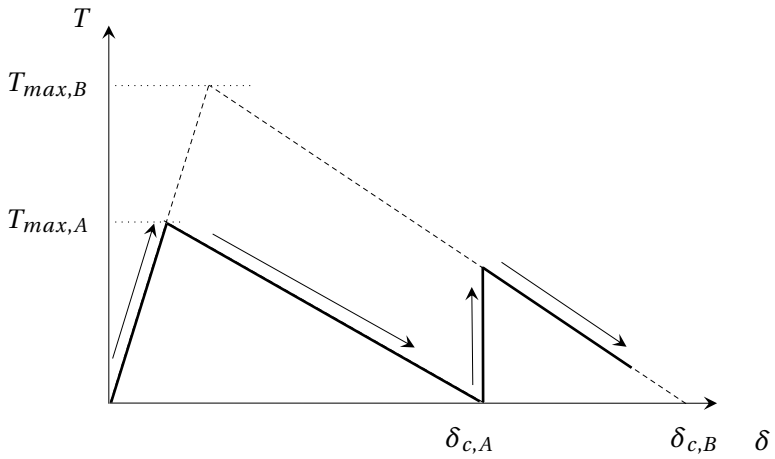


Figure 5.5: Displacement-based traction separation laws corresponding to two loading modes (mode A and mode B). The interface initially opens in mode A and the effective separation reaches the critical mode A separation $\delta_{c,A}$. Upon reaching a $\delta_{c,A}$, the loading mode is suddenly changed to mode B. The current effective displacement fallaciously corresponds to a not yet degraded mode B.

Potential-based models

Potential-based models are introduced to compensate for the shortcomings of the displacement-based models. The relationship of the tractions to normal and tangential displacements are obtained from a potential function (free energy). They may be based on interatomic potentials [119, 120], or other considerations [114, 121]. The use of a potential function from which to derive the traction is motivated by the dependence of the critical interface energy release rate on the mode-mixity. The first derivative of the potential with respect to either the normal or the tangential opening provides the normal and tangential traction respectively, the second derivative provides the material tangent required in the finite element calculations.

5.1.2 Cyclic cohesive zone models

The models described so far apply mostly to monotonic loading. In order to allow for cyclic loading, an additional unloading-reloading relation must be added to the formulation. Two possibilities are mentioned in the literature: either an elastic unloading, with a decrease of stiffness [122, 123] or an unloading featuring a residual separation with same stiffness as the initial stiffness [118] as shown in Fig. 5.3. Initially, the reloading was done on the same path as unloading. However, it was shown that it results in shakedown under constant amplitude loading and artificial crack arrest [99, 122, 124]. Thus a hysteretic unloading-reloading path is suggested [99, 125]. The hysteresis accounts for possible energy dissipation upon reloading due to *e.g.* the presence of asperities which may dissipate energy by friction.

5.2 Bouvard cyclic cohesive zone model

Using a contact formulation to implement a cohesive model solves the issue of the intrinsic thickness that is encountered when using interface element. Indeed, a crack segment has no thickness and thus representing it with an interface element that necessarily needs to be given a thickness is problematic in this sense. [126]

5.2.1 Bouvard model

The model presented here has been developed by Bouvard [126, 127] to model the damage localization for fatigue crack propagation. It is a potential-based model. The potential ϕ is

similar to the one-dimensional potential proposed by [128] and is given by:

$$\phi = \frac{1}{2}(1-D)K_N\left[\frac{\langle U_N\rangle^2}{\delta_c} + \alpha\frac{U_T^2}{\delta_c}\right] \tag{5.2}$$

where U_N and U_T are the normal and tangential separation in m, δ_c is a constant displacement value in m, K_N the initial stiffness in Pa and D the scalar damage variable monitoring damage accumulation. D varies between 0, *i.e.* the undamaged state and 1, *i.e.* the fully damage state. $\langle . \rangle$ are the Macauley brackets meaning $\langle x \rangle = x$ for $x \geq 0$ and $\langle x \rangle = 0$ for $x < 0$. It results in tractions being linear functions of the normal or tangential opening:

$$T_N = \frac{\partial \phi}{\partial U_N} = K_N(1-D)\frac{\langle U_N\rangle}{\delta_c} \tag{5.3}$$

$$T_T = \frac{\partial \phi}{\partial U_T} = \alpha K_N(1-D)\frac{U_T}{\delta_c} \tag{5.4}$$

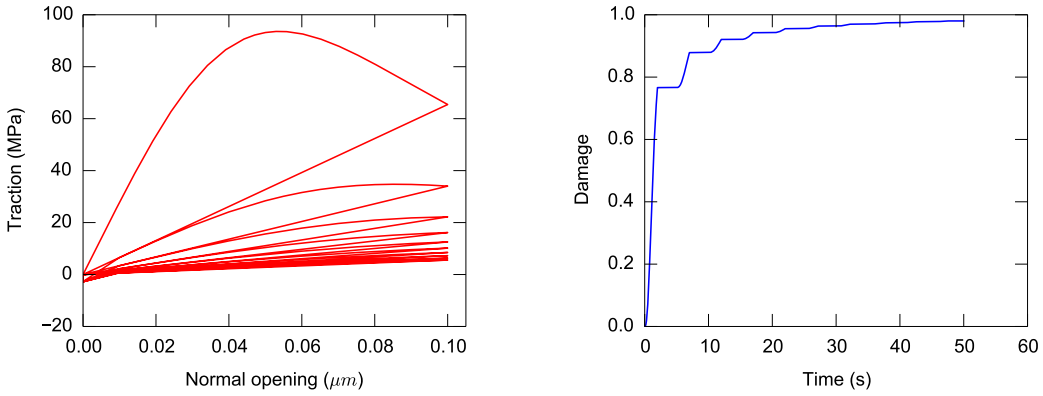
where T_N and T_T are the normal and tangential tractions in Pa respectively. $\alpha = K_N/K_T$ indicates the mode-mixity with respect to the mode I. $\alpha = 0$ means a pure mode I opening. The thermodynamical force resulting from the potential is given by its derivative with respect to the damage variable:

$$Y = -\frac{\partial \phi}{\partial D} = \frac{1}{2}K_N\left(\frac{\langle U_N\rangle^2}{\delta_c} + \alpha\frac{U_T^2}{\delta_c}\right). \tag{5.5}$$

It represents the elastic energy that could be stored if the interface was undamaged [128]. Thus its unit is Pa m or J m^{-2}. The parameters D and Y are internal variables of the model which account for the interface degradation. The state variable D can be interpreted as the effective surface density of microdefects in the interface [27, 118]. The evolution of D must be determined. Roe *et al.* [118] suggest to choose a damage evolution law depending on the normal opening, the tangential sliding and the current state of the damage variable:

$$\dot{D} = A^*(1-D)^m\left\langle \frac{\|T\|}{1-D} - T_0\right\rangle^n \|\dot{U}\| \tag{5.6}$$

where T_0 is the traction threshold, below which no damage occurs, A^* is a factor in Pa$^{-\mathrm{n}}$, m, n are dimensionless parameters of the model, $\|\dot{U}\|$ is the increment of effective separation such that $\|\dot{U}\| = \|U\|_t - \|U\|_{t-\Delta t}$. Note that $A^* = A\left[\delta_c/(2K_N)\right]^{n/2}$. The symbol $\|x\|$, where x is a vector with a normal component x_N and a tangential component x_T stands for $\sqrt{x_N^2 + x_T^2}$. The damage evolution law allows to account for cycling at subcritical loads. The damage variable D is history-dependent and integrates all the degradation processes that occur at the interface. Damage mechanics provides the tool to describe the progressive degradation of the interface.



(a) **(b)**

Figure 5.6: (a) Traction-separation curve showing unloading and reloading, as obtained from the Bouvard model. (b) Damage evolution during the cycling.

The effective traction $||T||$ is defined by:

$$||T|| = \sqrt{\langle T_N \rangle^2 + \frac{1}{\alpha} T_T^2} = K_N(1-D)||U|| \tag{5.7}$$

and the effective displacement:

$$||U|| = \sqrt{\left(\frac{\langle U_N \rangle}{\delta_c}\right)^2 + \alpha \left(\frac{U_T}{\delta_c}\right)^2}. \tag{5.8}$$

In case of crack closure, *i.e.* negative normal displacement, the following traction laws are enforced, for normal traction:

$$T_N = K_c \frac{U_N}{\delta_c}, \quad U_N < 0 \tag{5.9}$$

and for tangential traction:

$$T_T = \alpha K_N (1-D) \frac{U_T}{\delta_c}. \tag{5.10}$$

The damage evolution has the following characteristics, as expected from a damage evolution law [27]:

- damage starts to accumulate if the effective traction is above a threshold value,
- the increment of damage is linked to the increment of separation,
- damage occurs only during loading.

Frictionless contact is assumed between the crack lips, which may not be realistic, especially in the case of mode II loading.

Fig. 5.6 shows the traction-separation curve and damage evolution for a situation where the monotonic envelope is reached first and then a small load is cycled. Peak traction and stiffness degrade as damage accumulates. The inclusion of an unloading-reloading hysteresis within the cohesive law accounts for dissipative mechanisms likely to occur at the crack tip. As already discussed, the hysteresis prevents artificial crack arrest. The unloading takes place elastically.

5.2.2 Influence of the cohesive parameters

The size of the fracture process zone can be adjusted by varying the parameters K_N/δ_c and T_0, m controls the size of the wake zone. An increase of the threshold T_0 results in a smaller forward zone (where D ranges strictly from zero to one). The ratio K_N/δ_c controls the size of the fracture process zone, without being able to distinguish between the wake zone and the forward zone. [126]

Upon the proper choice of the parameters, additional constraints on their values must be observed. The value of m controls the wake zone *i.e.* the rate of softening of the traction-separation curve. Considering a simplification of the damage evolution law (Eq. 5.6) where $T_0 = 0$ and only normal displacements occur such that $||U|| = U_N/\delta_c$. For readability, U_N is denoted as U. Separating the variables and integrating between $[0, D]$ and $[0, U_N]$ gives:

$$\int_0^D \frac{dD}{(1-D)^m} = \frac{A^*}{\delta_c}\left(\frac{K_N}{\delta_c}\right)^n \int_0^U U^n dU \tag{5.11}$$

$$1 - D = \left[1 + \frac{A^*}{\delta_c}\left(\frac{K_N}{\delta_c}\right)^n \frac{m-1}{n+1} U^{n+1}\right]^{-\frac{1}{m-1}} \tag{5.12}$$

For values of m equal to one, the damage integration leads to a different law, which is not considered here. Two additional cases have to be studied:

- $m < 1$: the element fails when $D = 1$ but numerical divergence may happen. As a result, Bouvard chose to exclude this interval [126].
- $m > 1$ leads to an asymptotic behavior of damage. This is not a problem if a cut-off value of damage is given as model parameter. [126]

By considering the traction relation Eq. 5.3:

$$T = \frac{K_N}{\delta_c} U \left[1 + \frac{A^*}{\delta_c}\left(\frac{K_N}{\delta_c}\right)^n \frac{m-1}{n+1} U^{n+1}\right]^{-\frac{1}{m-1}} \tag{5.13}$$

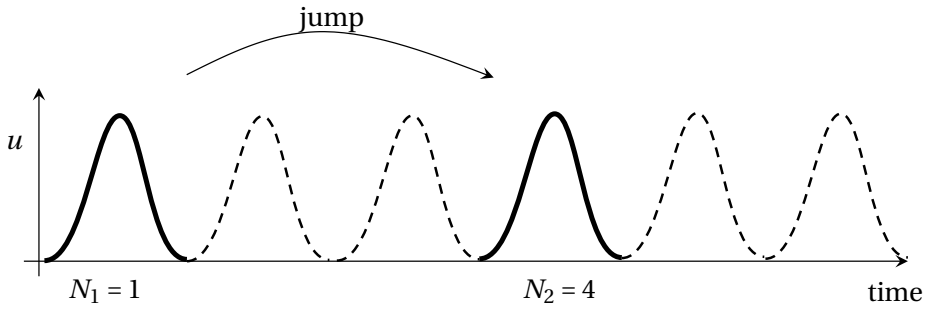


Figure 5.7: Cyclic jump technique (adapted from [130]).

and taking the limits for U going to infinity, the traction behavior is:

- if $\frac{n+1}{m-1} < 1$ then the traction tends to infinity when the separation tends to infinity,
- if $\frac{n+1}{m-1} = 1$ then the traction tends to a constant value,
- if $\frac{n+1}{m-1} > 1$ then the traction tends to zero when the separation tends to infinity.

To allow the element to fail with $T \to 0$, only $\frac{n+1}{m-1} > 1$ is allowed. This last case is the only physically admissible case.

Bouvard showed that, under certain simplifications, and assuming that the damage rate is proportional the crack growth rate, the parameters A and n of the model influence the Paris curve. A has an influence on the vertical offset of the Paris curve and n is linked to the slope. [126]

To calibrate the model, Bouvard proposes to first fix K_N and δ_c. The choice of K_N depends on numerical convergence arguments. Then the fracture process zone size must be found. As already discussed, it depends on K_N/δ_c, m and T_0. Using analytical expressions of the fracture process zone and a criterion involving ten elements in the plastic zone at the crack tip [129], the values of m and T_0 can be determined. The last step consists of calibrating A and n, as previously described. To summarize, calibrating the CZ model requires tests on the crack growth rate as well as observations on the size of the fracture process zone.

5.2.3 Cyclic jump technique

In case of cyclic loading with constant amplitude, the detailed computation of the structure on a cycle by cycle basis becomes computationally expensive when the number of cycles is large. Thus the concept of a cyclic jump procedure was introduced in damage mechanics [27]. A full block of cycles can be extrapolated based on the damage increment calculated during the last simulated cycle. Fig. 5.7 illustrates the principle. The cycles shown by solid lines are actually

simulated whereas the dashed lines depict cycles that are extrapolated. A direct iteration of the damage evolution law is performed [102, 131, 132]. Practically, it means that a specific routine is called at the end of a cycle and that the damage accumulation is calculated.

The damage value is computed for selected cycles N_0,N_1,...,N_n,N_{n+1} where $N_{n+1} - N_n$ corresponds to the cycle jump. The damage value at the cycle N_{n+1} D_{n+1} is calculated from the damage value at the cycle N_n D_n, the rate of damage change $(\partial D/\partial N)_n$ per cycle during the last calculated cycle N_n and the cycle jump $N_{n+1} - N_n$. [133]

$$D_{n+1} \approx D_n + \left(\frac{\partial D}{\partial N}\right)_n (N_{n+1} - N_n) \tag{5.14}$$

The cycle jump is chosen such that $D_{n+1} - D_n = \Delta D_{allow}$ is smaller than a limit chosen by the user. Small ΔD_{allow} allows for good accuracy, however at the expense of computational efficiency. A trade-off must be found here. At each new extrapolated cycle, a new damage value is calculated, while the displacements are still the ones calculated at the last simulated cycle. At the end of the extrapolation, a new damage value is obtained and this is taken as starting value for the next simulated cycle.

To avoid cases where the damage increment exceeds the maximum allowed damage increment per load increment due to a sudden increase of N_{n+1} compared to N_n, a more conservative approach is used:

$$N_{n+1} = N_n + \lambda (N_{n+1} - N_n) \quad \text{where } 0 \leq \lambda \leq 1. \tag{5.15}$$

5.3 Application example

5.3.1 Finite element model

Fig. 5.8 depicts the two-dimensional model of the package. The crack is assumed to grow along the interface between solder layer and the first barrier layer. The right side of the picture shows a zoom of the chip bottom, with the backside metalization and solder layers. To achieve convergence, a small bleedout is created on each side of the solder layer. Additionally, CZ elements are used along the vertical sidewall of the metalization layer located above the crack as well as along the bleedout. Otherwise, this location will create convergence difficulties due to the geometry and the material discontinuities.

The backside metalization layers are meshed with about two elements in the thickness direction *i.e.* the elements are regular quadrilaterals with a size of 150 nm. The solder layer is also meshed with such elements, except in the bleedouts where deformed quadrilaterals are al-

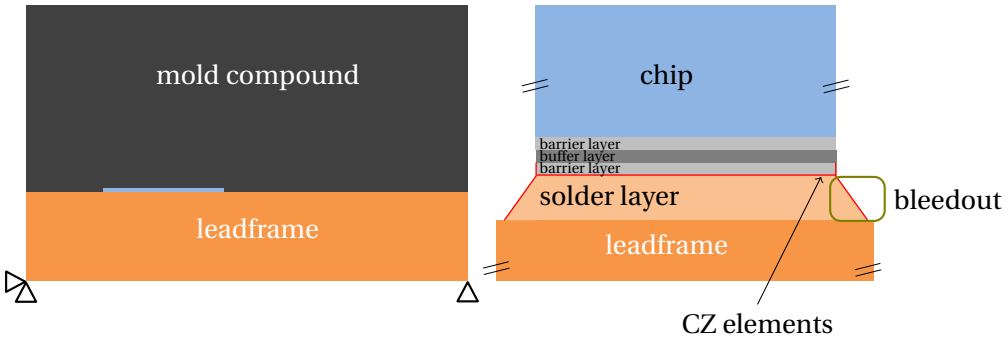


Figure 5.8: FE model. The left side shows the full geometry with the mechanical boundary conditions required to prevent rigid body motion. On the right side is a zoom of the bottom of the chip, where several backside metalization layers are visible as well as the solder. Small bleedouts have been implemented for convergence reasons.

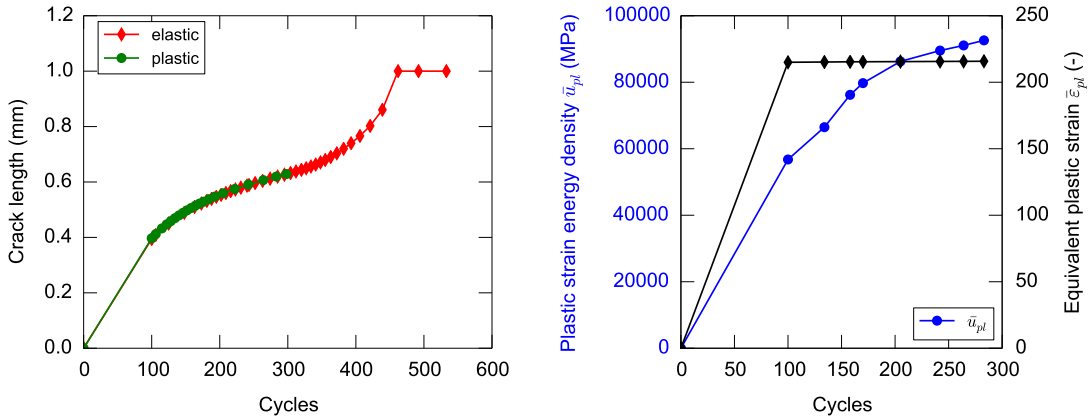
lowed. The solder and backside metalization layers add up to about $\frac{2}{3}$ of the total number of elements in the mesh. Transitions are used from the mold compound (element size of about 50 µm) down to the backside metalization.

Similar to the LEFM model, only the minimal mechanical boundary conditions are used. The thermal loading consists of a temperature uniformly applied on the whole model.

5.3.2 Crack growth evolution in cyclic loading

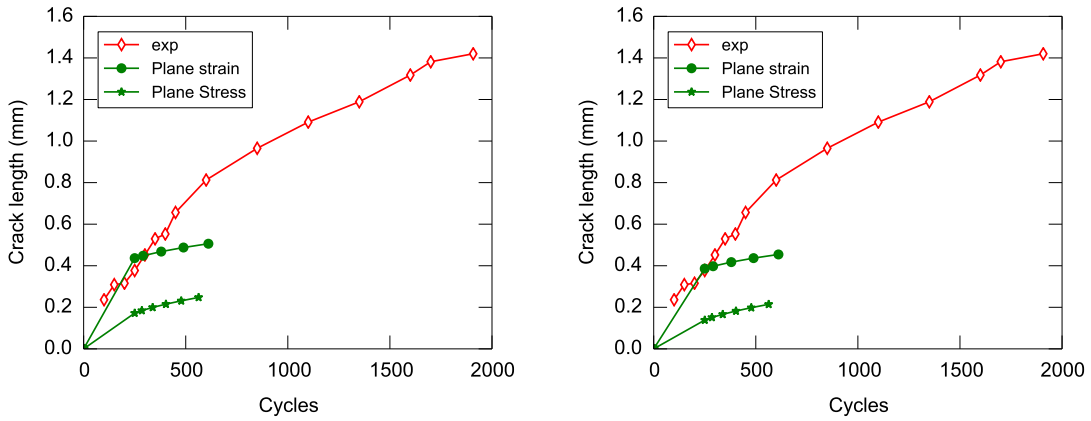
Fig. 5.9a shows the evolution of the crack length versus the number of thermal cycles between 50 °C to 200 °C. The chip is 1 mm-wide. The diamonds ♦ show the evolution when all the materials behave elastically while the bullets • represent the behavior of the system when the plasticity is taken into account. The large number of cycles is simulated using the cyclic jump technique. The crack length depends on the number of cycles following a power law for cycles between 0 to 300. Due to the chosen properties of the cohesive zone interface, the crack propagates after a very short number of cycles toward the center of the chip. At 300 cycles, the crack has already reached the middle of the chip. The plasticity of the solder layer has in the present case no influence on the crack growth as elastic and plastic cases exhibit the same behavior. Plasticity does not cause crack closure phenomena.

Fig. 5.9b shows the evolution of the plastic strain energy density and the equivalent plastic strain in the solder layer with the number of cycles. The plastic strain grows very fast in the first cycles, which corresponds to initial damage and then grows very slowly. The plastic strain energy density grows non-linearly with the number of cycles. Its initial growth is fast. The plastic strain energy density could be taken as a damage indicator for degradation into the solder layer.



(a) **(b)**

Figure 5.9: (a) Crack length versus the number of cycles for a chip of 1 mm length, for the case of fully elastic materials (elastic) and taking into account plasticity (plastic). (b) Equivalent plastic strain and plastic strain energy density summed over the solder layer.



(a) **(b)**

Figure 5.10: Crack length versus the number of cycles for a chip of 1.5 mm length. The measured data are compared with simulated data, for two cases: plane strain and plane stress. (a) for the crack located on the left side of the chip.(b) for the crack located on the right side of the chip.

5.3.3 Results and discussion

Fig. 5.10 shows the crack length versus the number of thermal cycles for two simulated stress conditions (color-filled symbols) and compare them to the experimental results (white-filled symbols). The chip is 1.5 mm wide. As the experimental data is collected on an area basis with an assumption on the shape of the delaminated area, it is expected that the experimental curve is located in between the plane stress and plane strain conditions curves. Here the expectation is not fulfilled as the calibration is performed on the basis of the left crack results. For both left and right cracks, plane strain condition is the worst case *i.e.* it leads to a faster initial crack growth compared to plane stress. Plane stress results are almost identical for both crack locations. Plane strain results exhibit an initial crack growth which is slightly faster when considering the left crack. This does not agree with experimental findings, as a rectangular chip delaminates more severely on the right side while no influence is observed for square chip. This hints to an influence of the third dimension of the package that would have to be considered using a three-dimensional FE model.

6

Conclusion

In this work, the problem of the degradation of the die-attach layer in a package is treated. The reliability of semiconductor components is crucial for numerous applications *e.g.* in the automotive industry. In addition, the lifetime of the components must comply with some requirements to ensure the quality of the devices. Semiconductor components are complex structures with interactions between the electrical, thermal and mechanical aspects. The problem is approached from two perspectives, *i.e.* using both simulation and experiments. Several issues have to be considered, such as the validity of using a continuum approach to model thin film materials or the capability of transferring methods developed for large scale degradation down to small scale.

Electronic devices contain numerous thin metalization layers, whose properties might be unknown. A methodology for obtaining a model for the material behavior of thin films has been developed. The literature clearly indicates that a coupling between thickness and microstructure effects is responsible for the behavior of thin films. Thin films are reported to have a much larger yield stress than their bulk counterpart. Their elastic properties are also influenced, generally leading to a lower Young's modulus due to the presence of defects. Continuum models have been reported to capture at least partially the behavior of thin films and are thus used in subsequent finite element simulations to study the stress states in electronic devices. Curvature measurements are used for this work. The material model is fitted to the experimental data. They can be considered as valid in the range of conditions where the experiments have

been performed. It serves as a first good approximation to be used in subsequent finite element simulations, as it takes into account some particularities of the thin film behavior instead of directly using the bulk material data. In this work, the continuum mechanics approach is sufficient to describe the experimental data.

One issue in electronics packaging is that the very complex structure and long expected lifetime make it difficult to monitor crack propagation. Current practice is to use accelerated testing, to induce failure in a shorter amount of time. The main issue is to ensure that the use of acceleration factors like temperature does not trigger any additional or different failure mechanism. In this work, a test has been developed to accelerate degradation using temperature as acceleration factor. The devices are placed on a power resistor that is used as a heating plate. It is shown that this test induces degradation of the solder layer 8 times faster than a standard temperature cycling test, while triggering the same failure mode. Non-destructive punctual monitoring of the die-attach layer revealed a crack growing according to a power law of the number of cycles. Additionally the crack growth rate is a decreasing exponential law of the number of cycles. This typical crack growth behavior is used for qualitative comparison in the subsequent simulation.

To understand which parameters are important for the geometry and the material, the LEFM approach is used to qualitatively compare the trends observed in experiments and simulation. This kind of study allows for a first approximation of the important parameters once the failure mechanisms and failure modes are known. The energy release rate has been chosen as fracture parameter to monitor the crack growth. This parameter is still valid for evaluating interfacial crack propagation.

A Cohesive Zone (CZ) approach is used here to model the degradation of the interface. A model incorporating progressive damage due to fatigue is considered. Thanks to the cyclic jump technique, computation time can be reduced even for computation of a large number of cycles in temperature cycling. It is shown that for the particular combination of materials, the presence of plasticity in the layers surrounding the crack does not have a strong influence on the crack growth. However, the plastic strain energy density in the solder layer can be related to degradation. The crack length is shown to follow a power law of the number of cycles, as expected from the experimental data. The material data for the CZ model have to be calibrated with the available experiments. Direct measurements would require the design of a specific set of samples and experiments.

Degradation of the solder layer in a package is a crucial topic nowadays in the semiconductor industry. Indeed, it appears that the package is increasingly impacting the chip performance as they tend towards smaller sizes and larger current densities. As a result thermomechanical reliability has become a vital issue for proper functioning and lifetime of the devices. A common research problem in the industry is to change the backside metalization layer or the solder layer

without having to actually build prototypes, as this is time-consuming, *i.e.* up to three months for the prototypes fabrication. Furthermore, they may not be built under the same conditions or with exactly the same materials as in production, thus leading to erroneous conclusions. Simulation is a possible solution to investigate such problems. In this work, new methods to model package and failure mechanisms have been presented. The results agree well with actual experimental data. In the upcoming years with an increasing amount of computing power, it will be possible to simulate numerous complex layer structures.

With the growing demands on the package's performance, new packages are developed whose failure modes have to be identified. Standard tests are still widely used. However one has to bear in mind that these standard test do not always correspond the loading seen by the device in application. This work has shown that using simulation with an appropriate model makes it possible to simulate the actual mission profile seen by the devices for an arbitrarily complex layer set-up.

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Acronyms

AuSn	gold-tin.
CTE	Coefficient of Thermal Expansion.
Cu	copper.
CVD	Chemical Vapor Deposition.
CZ	Cohesive Zone.
DAQ	Data Acquisition.
DIP	Dual-In-Line.
DUT	Device Under Test.
FE	Finite Element.
FIB	Focused Ion Beam.
HTRB	High Temperature Reverse Bias.
IOL	Intermittent Operating Life.
IRT	InfraRed Thermography.
LEFM	Linear Elastic Fracture Mechanics.
LTSL	Low Temperature Storage Life.
PCB	Printed Circuit Board.
PGA	Pin Grid Array.
PLCC	Plastic Leaded Chip Carrier.
PVD	Physical Vapor Deposition.
QFP	Quad Flat Pack.
SAM	Scanning Acoustic Microscopy.

SEM	Scanning Electron Microscope.
Si	Silicon.
SiC	Silicon Carbide.
SMU	Source Measurement Unit.
SO	Small Outline.
SOT	Small Outline Transistor.
TC	Temperature Cycling.
TO	Transistor-Outline.
TSL	Traction-Separation Law.

Symbols

T_{HIGH}	Maximum temperature during a cycle.
T_{LOW}	Minimum temperature during a cycle.